

From Silicon to Physical Intelligence:
Heterogeneous SoC Innovations



ISOCC 2026

23rd International SoC Design Conference

October 11-14, 2026
Songdo ConvensiA, Incheon, Korea



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PROGRAM BOOK

*“From Silicon to Physical Intelligence:
Heterogeneous SoC Innovations”*



ISOCC 2026

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ISOCC 2026
23rd International SoC Design Conference

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FOREWORD

Welcome to ISOCC 2026, and welcome to Incheon!

It is my great pleasure to welcome you to the 23rd International SoC Design Conference (ISOCC 2026), held from October 11 to 14, 2026, at Songdo ConvensiA in Incheon, Korea.

Over the years, ISOCC has established itself as an important international forum where researchers, engineers, and industry leaders from around the world come together to share research advances, exchange ideas, and explore emerging directions in System-on-Chip (SoC) design.

Under this year's theme, "From Silicon to Physical Intelligence: Heterogeneous SoC Innovations," ISOCC 2026 highlights the evolving role of SoC technologies in bridging advances in silicon with intelligent systems that sense, interact with, and respond to the physical world. The theme reflects the growing importance of heterogeneous integration and innovative SoC architectures in enabling the next generation of intelligent systems.

ISOCC 2026 features a diverse technical program, including plenary speeches, invited talks, tutorials, technical paper presentations, special sessions, the Chip Design Contest, and various networking and social events. We hope these programs will inspire new ideas, encourage meaningful discussions, and foster new collaborations across academia and industry.

Our host city, Incheon, is Korea's international gateway and a dynamic city where technology, business, culture, and waterfront scenery come together. Songdo, home to the conference venue, offers convenient access from Incheon International Airport and a modern environment for international exchange. We hope you will also take the opportunity to experience the unique attractions and warm hospitality of Incheon during your stay.

I would like to express my sincere appreciation to the Organizing Committee, Technical Program Committee, Steering Committee, reviewers, session organizers, speakers, authors, sponsors, and supporters whose dedication and contributions have made ISOCC 2026 possible.

Most importantly, I extend my warmest welcome and sincere gratitude to all participants joining us from around the world. I hope ISOCC 2026 will provide you with inspiring technical discussions, valuable new connections, and memorable experiences.

Youngmin Kim
General Chair, ISOCC 2026

MESSAGE FROM TPC CHAIR

On behalf of the Technical Program Committee, it is our pleasure to welcome you to the 23rd International SoC Design Conference (ISOCC 2026) in Incheon, Korea. ISOCC continues our tradition of showcasing the latest innovations and advancements in the System-on-Chip (SoC) area. This year, the conference theme is “From Silicon to Physical Intelligence: Heterogeneous SoC Innovations”. Over the past decade, technology has evolved rapidly, and SoC technologies have been at the forefront of this evolution, driving advancements across diverse fields such as machine learning, AI architectures, advanced packaging, and physical AI systems. ISOCC 2026 aims to highlight the latest technological breakthroughs that will shape the future of our society.

The ISOCC 2026 technical program features 181 outstanding papers across 25 technical sessions. This includes 153 regular papers presented in oral and poster sessions, as well as 28 special session papers. The selected papers represent a competitive and international pool of submissions, reflecting the global reach and impact of this conference. Following our successful traditions, we are proud to continue key programs including the Special Sessions, the Undergraduate Research Exhibition Fair (U-REF), and the Chip Design Contest (CDC), providing an invaluable opportunity for researchers, industry experts, and the younger generation to share fresh ideas and collaborative solutions.

The conference is honored to host insightful keynote speeches by leading innovators from both academia and industry. Additionally, ISOCC 2026 includes educational tutorials designed to foster knowledge sharing and collaboration in SoC research and development. I would like to extend my sincere gratitude to all contributors to the technical program, including authors, reviewers, special session organizers, organizing committee members, and technical program committee members. Your dedication and hard work are what make ISOCC 2026 possible. We hope that the technical program will be enjoyable and rewarding for all participants.

Ilku Nam

Technical Program Committee Chair, ISOCC 2026

Yoko Uwate

Technical Program Committee Co-Chair, ISOCC 2026

INVITATION TO ISOCC 2027

It is my great pleasure to invite you to the 24th International SoC Design Conference (ISOCC 2027), which will be held in Kobe, Japan. Building upon more than two decades of successful gatherings, ISOCC continues to serve as an international forum where researchers, engineers, and industry professionals share the latest advances and explore new directions in System-on-Chip (SoC) design and semiconductor technologies.

ISOCC 2027 will bring together leading researchers and professionals from academia, industry, and research institutes to discuss emerging opportunities and challenges in next-generation semiconductor systems. Under the theme “AI-Driven SoC Innovation: From Intelligent Design to Intelligent Systems”, the conference will highlight technological innovations shaping the future of SoC design, from advanced integrated circuits and heterogeneous systems to AI computing, AI-based design automation, and emerging semiconductor technologies.

Kobe, one of Japan’s leading international port cities, offers a distinctive combination of advanced urban infrastructure, rich culture, and beautiful scenery between the Rokko Mountains and Osaka Bay. With convenient transportation connections to major cities and international airports in the Kansai region, Kobe provides an excellent setting for academic exchange and international collaboration. We hope participants will also enjoy the city’s unique atmosphere, cuisine, waterfront, and cultural attractions during their stay.

The ISOCC 2027 program will feature keynote speeches, invited talks, tutorials, technical paper sessions, special sessions, and a variety of opportunities for technical exchange and networking. We look forward to welcoming researchers and professionals from around the world and creating another memorable chapter in the history of ISOCC.

On behalf of the ISOCC 2027 Organizing Committee, I warmly invite you to join us in Kobe, Japan. We look forward to sharing new ideas, building meaningful collaborations, and advancing the future of SoC technologies together at ISOCC 2027.

See you in Kobe!

Minkyu Je
General Chair, ISOCC 2027

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TIME TABLE

SUNDAY_ OCTOBER 11, 2026

	LOBBY	201+202	204	205	206	207
12:30 - 13:00	On-site Registration					
13:00 - 14:30		Main Tutorial 1				
14:30 - 15:10		Short Tutorial 1				
15:10 - 15:20		Break Time (10 min.)				
15:20 - 16:50		Main Tutorial 2				
16:50 - 17:30		Short Tutorial 2				

MONDAY_ OCTOBER 12, 2026

	LOBBY		201+202		204		205		206		207		
8:40 – 8:55	On-site Registration	Chip Design Contest (CDC) Poster	CDC Oral	CDC ~D01									
8:55 – 9:10				CDC ~D02									
9:10 – 9:25				CDC ~D03									
9:25 – 9:40				CDC ~D04									
9:40 – 9:55				CDC ~D05									
9:55 – 10:10				CDC ~D06									
10:10 – 10:15			Short Break (5 min.)										
10:15 – 10:30			Opening Ceremony (Premier Ballroom)										
10:30 – 11:20			Keynote Speech–1 (Premier Ballroom)										
11:20 – 11:30			Break Time (10 min.)										
11:30 – 12:20			Keynote Speech–2 (Premier Ballroom)										
12:20 – 13:40			Sponsor Exhibition	CDC Demo Sessions	Lunch (80 Min.)								
13:40 – 13:55					MLAI 1 p. 36	210	SoC 1 p. 37	92	DCA 1 p. 38	20	AC 1 p. 39	47	WICAS p. 24
13:55 – 14:10		111				176		110		222			
14:10 – 14:25		21				25		139		173			
14:25 – 14:40		10				186		240					
14:40 – 14:55		151											
14:55 – 15:10	Break Time (15 min.)												
15:10 – 15:25			MLAI 2 p. 40	179	SoC 2 p. 41	37	DCAS 2 p. 42	16	SS 1 p. 56	300	SS 2 p. 58	15	
15:25 – 15:40				5		69		144		299		17	
15:40 – 15:55				200		81		148		298		18	
15:55 – 16:10				103		39		216		303		38	
16:10 – 16:25				147				241		302		65	
16:25 – 16:40										304		180	
16:40 – 16:55	Break Time (15 min.)												
16:55 – 17:40	CDC Poster Exhibition												
17:40 – 18:00	Break Time (20 min.)												
18:00 – 20:00	Banquet (Premier Ballroom A+B)												

TIME TABLE

TUESDAY _ OCTOBER 13, 2026

	LOBBY		201+202	204	205	206	207																														
9:00 – 9:15	On-site Registration Sponsor Exhibition	Regular Paper Poster	MLAI 3 p. 43	<table><tr><td>122</td></tr><tr><td>112</td></tr><tr><td>83</td></tr></table>	122	112	83	AC/WL p. 44	<table><tr><td>182</td></tr><tr><td>60</td></tr><tr><td>207</td></tr><tr><td>14</td></tr></table>	182	60	207	14	ET 1 p. 45	<table><tr><td>3</td></tr><tr><td>51</td></tr><tr><td>79</td></tr><tr><td>174</td></tr></table>	3	51	79	174	AC 2 p. 46	<table><tr><td>293</td></tr><tr><td>4</td></tr><tr><td>136</td></tr><tr><td>211</td></tr></table>	293	4	136	211	RF 1 p. 47	<table><tr><td>7</td></tr><tr><td>137</td></tr><tr><td>26</td></tr><tr><td>133</td></tr></table>	7	137	26	133						
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10:10 – 11:00	Keynote Speech–3																																				
11:00 – 11:10	Break Time (10 min.)																																				
11:10 – 12:00	Keynote Speech–4																																				
12:00 – 13:20	Lunch (80 Min.)																																				
13:20 – 13:35			DC 1 p. 48	<table><tr><td>117</td></tr><tr><td>128</td></tr><tr><td>73</td></tr><tr><td>291</td></tr><tr><td>196</td></tr></table>	117	128	73	291	196	SoC 3 p. 49	<table><tr><td>205</td></tr><tr><td>150</td></tr><tr><td>194</td></tr><tr><td>30</td></tr><tr><td>219</td></tr></table>	205	150	194	30	219	ET 2 p. 50	<table><tr><td>70</td></tr><tr><td>80</td></tr><tr><td>42</td></tr><tr><td>140</td></tr></table>	70	80	42	140	RF 2 p. 51	<table><tr><td>28</td></tr><tr><td>201</td></tr><tr><td>95</td></tr><tr><td>12</td></tr><tr><td>198</td></tr></table>	28	201	95	12	198	SS 3 p. 60	<table><tr><td>87</td></tr><tr><td>220</td></tr><tr><td>292</td></tr><tr><td>296</td></tr></table>	87	220	292	296		
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14:35 – 14:50	Break Time (15 min.)																																				
14:50 – 15:05			MLAI 4 p. 52	<table><tr><td>109</td></tr><tr><td>119</td></tr><tr><td>98</td></tr><tr><td>204</td></tr><tr><td>50</td></tr></table>	109	119	98	204	50	WL p. 53	<table><tr><td>197</td></tr><tr><td>155</td></tr><tr><td>48</td></tr><tr><td>206</td></tr><tr><td>61</td></tr></table>	197	155	48	206	61	DCAS 3 p. 54	<table><tr><td>13</td></tr><tr><td>62</td></tr><tr><td>72</td></tr><tr><td>138</td></tr><tr><td>209</td></tr></table>	13	62	72	138	209	SS 4 p. 62	<table><tr><td>11</td></tr><tr><td>67</td></tr><tr><td>91</td></tr><tr><td>108</td></tr><tr><td>175</td></tr></table>	11	67	91	108	175	SS 5 p. 64	<table><tr><td>33</td></tr><tr><td>86</td></tr><tr><td>89</td></tr><tr><td>99</td></tr><tr><td>102,104</td></tr></table>	33	86	89	99	102,104
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15:50 – 16:05																																					
16:05 – 16:45	Regular Papers Poster Exhibition																																				
16:45 – 17:00	Break Time (15 min.)																																				
17:00 – 17:30	Closing Ceremony (Premier Ballroom)																																				

WEDNESDAY _OCTOBER 14, 2026

10:00 - 11:00	Committee Meeting & Discussion		
ML/AI session 1	LLM Acceleration and Efficient Transformer Inference	Analog Circuits session 2	Analog Techniques
SoC session 1	AI-Driven EDA and Design Optimization	RF/Wireless session 1	Advanced Frequency Generation and Synthesis Circuits
DCAS session 1	Arithmetic and Computing Architectures	Data Converters session 1	High-Speed and High-Resolution Data Converters
Analog Circuits session 1	Power Management Circuits	SoC session 3	Hardware Security, Test, and Reliability
ML/AI session 2	AI Accelerator Architectures and FPGA Implementations	RF/Wireless session 2	RF Front-end Circuits and Wireless Systems
SoC session 2	Physical Design, Thermal, and Manufacturing Methodologies	ET session 2	Circuits & Systems for Emerging Applications
DCAS session 2	Communication and Signal Processing Systems	ML/AI session 4	Efficient AI Computing: Quantization, Pruning, and Neuromorphic Computing
ML/AI session 3	Edge AI Applications and Efficient Vision Systems	Wireline session 1	Advanced Wireline Transceivers and Clocking Techniques
Analog+Wireline session	Integrated Circuits for Next-Generation Communication and Energy-Efficient Systems	DCAS session 3	Memory and In-Memory Computing Systems
ET session 1	Emerging Technologies for Advanced Computing		

MAIN TUTORIAL

MAIN TUTORIAL

SUNDAY, OCTOBER 11, 2026

Main Tutorial 1

Chair : Prof. Younghyun Lim (Kyung Hee University, Korea)

13:00~14:30, SUNDAY_OCTOBER 11, 2026
201+202 (2F)

PUF-Based Hardware Security: Architectures, Attacks, and Countermeasures

Prof. Ambika Prasad Shah

*Associate Professor, School of Electrical Engineering,
Indian Institute of Technology Jammu, India*



Biography

Dr. Ambika Prasad Shah is currently working as an Associate Professor in the Electrical Engineering Department and Associate Dean Administrative Affairs at the Indian Institute of Technology Jammu, India. He received Ph.D. degree from the Electrical Engineering Department, Indian Institute of Technology Indore, India. Before joining IIT Jammu, Dr. Shah worked as a Postdoctoral Fellow at the Institute for Microelectronics, TU Vienna, Austria. He is the recipient of the Young Scientist Award from the M.P. Council of Science and Technology Bhopal, M.P. India. He received a Young Faculty Research Fellowship (YFRF) from the Ministry of Electronics and Information Technology (MeitY), Government of India in 2025. He was nominated for the 10th BRICS Young Scientist Forum 2025 in Brazil by DST, Govt. of India. He is the recipient of the Best Paper Award for two consecutive years at the 28th International Symposium on VLSI Design and Test (VDAT) 2024 and 29th International Symposium on VLSI Design and Test VDAT 2025, Second Best Award at the 7th International Conference on Microelectronics, Circuits and Systems (Micro 2020), and was nominated for the Best Paper from 31st IEEE Conference on Very Large Scale Integration (VLSI SoC 2023).

MAIN TUTORIAL

Abstract

The increasing use of electronic systems in applications such as aerospace, defense, healthcare, and the Internet of Things (IoT) has made hardware security an essential requirement. Software based techniques alone are often not sufficient to protect systems against physical attacks, reverse engineering, and side channel threats. This has led to the development of hardware security primitives that provide intrinsic security at the device level. Among these, Physically Unclonable Functions (PUFs) have gained significant attention due to their ability to generate unique and device specific signatures based on manufacturing variations. This tutorial, titled “PUF Based Hardware Security: Architectures, Attacks, and Countermeasures,” presents a structured overview of PUFs and related hardware security techniques. It begins with an introduction to hardware security primitives, highlighting their role in establishing trust in integrated circuits. The concept of PUFs is then introduced, explaining how process variations can be used to generate unpredictable yet repeatable responses. The tutorial covers the classification of PUFs into weak and strong types, based on their challenge response behavior and application requirements.

A detailed discussion on commonly used PUF architectures is included, such as SRAM PUFs, Ring Oscillator (RO) PUFs, Arbiter PUFs, and latch based PUFs. For each type, the design principles, advantages, limitations, and practical considerations are explained. The tutorial also addresses the modeling of PUF behavior, which is important for understanding both their functionality and potential vulnerabilities. To evaluate the effectiveness of PUFs, several performance metrics are discussed in detail, including uniqueness, reliability, randomness, bit error rate (BER), key error rate (KER), and uniformity. These metrics provide a quantitative basis for comparing different PUF designs and assessing their suitability for specific applications.

In addition to PUFs, the tutorial covers related hardware security techniques such as hardware metering and IC authentication, which are important for protecting the semiconductor supply chain and preventing counterfeiting. Logic locking and hardware obfuscation methods are also discussed, focusing on how they can be used to protect intellectual property and restrict unauthorized use of integrated circuits.

The tutorial further explores the application of hardware security primitives in trusted systems, including secure key generation, device authentication, and protection of sensitive data. Examples from practical domains such as embedded systems, biomedical devices, and space electronics are considered to provide context for real world implementation. A significant part of the tutorial is dedicated to the analysis of attacks on PUF based systems. Machine learning based modeling attacks are examined to show how attackers can predict PUF responses under certain conditions. In addition, electromagnetic (EM) side channel attacks are discussed, with an emphasis on their impact on hardware security primitives.

Finally, the tutorial presents various countermeasures to improve the robustness of PUFs and related systems. These include design techniques, architectural modifications, and methods to reduce side channel leakage and modeling vulnerability. The tutorial is intended for researchers, engineers, and graduate students working in VLSI design and hardware security, and aims to provide both fundamental understanding and practical insights for secure hardware design.

MAIN TUTORIAL

Main Tutorial 2

Chair : Prof. Min-Jae Seo (University of Seoul, Korea)

15:20~16:50, SUNDAY_OCTOBER 11, 2026
201+202 (2F)

Building Neural Interfaces – Key Components, System Integration, and Technical Hurdles

Prof. Minkyu Je

*Professor,
Korea Advanced Institute of Science & Technology (KAIST), Korea*



Biography

Minkyu Je is currently a Professor in the School of Electrical Engineering at KAIST, Daejeon, Korea. He received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from KAIST in 1996, 1998, and 2003, respectively.

Prior to his current position, Prof. Je gained extensive industry and research institute experience. He served as a Senior Engineer at Samsung Electronics (2003–2006) and later joined the Institute of Microelectronics (IME), A*STAR, Singapore, where he led the Integrated Circuits and Systems Laboratory as a Department Head and served as the Program Director of the NeuroDevices Program (2006–2014). Before returning to KAIST in 2016, he was an Associate Professor at DGIST, Korea (2014–2016).

His research focuses on developing advanced IC platforms for smart sensor interfaces, low-power wireless communication, high-efficiency energy supply and management, low-power timing, and resource-constrained computing. He actively integrates these technologies into microsystems for emerging applications, including intelligent biomedical devices, ubiquitous wireless sensor nodes, and next-generation mobile systems.

He has authored over 470 publications, edited one book, and holds more than 80 patents. He has served on the TPC for ISSCC, SOVC, and A-SSCC. He was an IEEE CASS Distinguished Lecturer and is now an IEEE SSCS Distinguished Lecturer. He is also serving as an Associate Editor of IEEE TBioCAS. He was awarded the Haedong Semiconductor Engineering Award in 2022 and received the Ministerial Commendation from the Ministry of Science and ICT in 2024.

MAIN TUTORIAL

Abstract

This presentation provides a comprehensive overview of building advanced implantable neural interfaces, focusing on neurotherapeutic and neuroprosthetic applications. It details the generic system-on-chip structure, comprising neural front-ends, signal processing, wireless power transfer, and data communication. It also addresses critical component-level challenges, such as achieving low-noise recording and high-efficacy stimulation, alongside system integration hurdles like miniaturization and data up-scaling.

SHORT TUTORIAL

SHORT TUTORIAL

SUNDAY, OCTOBER 11, 2026

Short Tutorial 1

Chair : Prof. Min-Jae Seo (University of Seoul, Korea)

14:30~15:10, SUNDAY_OCTOBER 11, 2026
201+202 (2F)

Biomedical analog front-ends techniques for bio-signal acquisition

Prof. Kyeongwon Jeong

*Associate Professor, School of Integrated Technology,
Yonsei University, Korea*



Biography

Kyeongwon Jeong (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2015 and 2018, respectively, and the Ph.D. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea. From 2023 to 2026, he was a Post-Doctoral Researcher at ETH Zurich, Zurich, Switzerland. Since 2026, he has been an Assistant Professor at Yonsei University, Incheon, South Korea, where he leads the Power-Efficient Intelligent Circuit and System Laboratory. He has published 3 papers in the IEEE Journal of Solid-State Circuits (JSSC) and 1 in the IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) as the first author. Furthermore, he has presented 4 conference papers, including ISSCC, VLSI, CICC, and A-SSCC.

SHORT TUTORIAL

Abstract

With the rapidly growing demand for healthcare monitoring, securing high-quality physiological signals (e.g., ECG, EMG, EOG, and EEG) has become essential, yet it faces severe obstacles such as circuit noise, electrode DC offset, high micro-electrode impedance, and massive stimulation or motion artifacts up to 100mVPP. To ensure reliable signal acquisition, biomedical analog front-ends (AFEs) must satisfy stringent requirements, including a low noise efficiency factor (NEF), wide dynamic range (DR), high common-mode rejection ratio (CMRR), and high input impedance. This tutorial provides a comprehensive overview of biomedical AFEs, beginning with a detailed explanation of key specifications derived from physiological signal characteristics and acquisition challenges. We will extensively review conventional topologies, tracking the evolutionary path from traditional low-noise amplifier (LNA)-first architectures—which suffer from limited DR and saturation under large artifacts—to contemporary continuous-time delta-sigma modulator (CT-DSM) direct-digitization schemes that are inherently limited by degraded NEF due to high noise-gain constraints. Finally, we introduce an advanced direct-digitization technique featuring Delta-Amplification (DA) and feedback cancellation integrated with noise-shaping SAR (NS-SAR) ADCs, presenting a key design methodology to break the conventional trade-off between noise performance and linear dynamic range for next-generation, artifact-tolerant biomedical system designs.

SHORT TUTORIAL

Short Tutorial 2

Chair : Prof. Minyoung Song (DGIST, Korea)

16:50~17:30, SUNDAY_OCTOBER 11, 2026
201+202 (2F)

Ultra-Low Power Neuromorphic System-on-Chip: From Concept to Product

Prof. Amir Zjajo

*Chief Scientific Officer,
Innatera Nanosystems B.V., The Netherlands*



Biography

Amir Zjajo is co-founder of Innatera Nanosystems B.V. and serves as its Chief Scientist. Prior to that, he was a member of research staff in the Mixed Signal Circuits and Systems Group at Philips Research Laboratories between 2000 and 2006, and subsequently, with Corporate Research at NXP Semiconductors until 2009. He joined the Delft University of Technology the same year and was responsible for leading research into a range of intelligent systems. Dr. Zjajo has published 3 books, more than 100 papers in referenced journals and conference proceedings in the areas of mixed-signal VLSI design, and neuromorphic circuits and systems, and holds more than 25 US patents or patent pending. He served as a TPC member of ISQED, DATE, VLSI Symposium, ISCAS, and BioCAS, among others. He received the M.Sc. and DIC degrees from the Imperial College London, London, U.K., in 2000, and the PhD. degree from Eindhoven University of Technology, Eindhoven, The Netherlands in 2010, all in electrical engineering. His research interests include energy-efficient mixed-signal circuit and system design for neuromorphic signal processing and inference, and bionic electronic circuits for autonomous cognitive systems. Dr. Zjajo won best/excellence paper award at BioDevices'15, LifeTech'19 and AICAS'23. He is a senior member of IEEE.

SHORT TUTORIAL

Abstract

Sensor content in electronic devices is growing, and an increasing number of applications involve battery-powered devices. The application of sensors is typically always-on, and this requires large power efficiency within the sense-process-act chain. However, today, the processors available for handling sensors and processing sensor data are characterized by high power-per-inference consumption. Much of the inefficiency lies within how sensor data is acquired from sensors, and how the information is relayed within processing sub-systems. Advanced, next generation neuromorphic processors, aim to deliver a novel data processing pipeline in which all signal processing, compute, and AI functionalities are integrated within an energy-efficient heterogeneous computing fabric, allowing for fast, ultralow power processing of sensor data on-device.

In this tutorial, we examine the entire design process, from the initial, biologically inspired computational concepts, via the silicon-prototype development and concurrent hardware-software co-design, to the product-level ready system-on-chip validated across multiple wafers. In addition to an accelerator capability to recognize patterns, we highlight novel architectural solutions that extend typical signal processing pipelines to encompass adaptive active sensing and enable reactive and predictive system-on-chip energy-aware control. The tutorial delves into the contemporary trends of neuromorphic computing, explore its capabilities and challenges, and contemplate its future directions and broader impact within the AI community and industry. The target audience includes research students, early-stage researchers, and practitioners with a background in SoC and AI.

WiCAS SESSION

WICAS SESSION

MONDAY, OCTOBER 12

WiCAS 1

Chair: Sunghye Park (Ajou University, Korea)

13:40~14:10, MONDAY_OCTOBER 12, 2026
207 (2F)

Toward AI-Driven Analog Circuit Design: From LLM-Based Refinement to Device-Level Topology Generation

Yulhwa Kim

*Assistant Professor, Department of Semiconductor Systems Engineering,
Sungkyunkwan University, Korea*



Biography

Yulhwa Kim received the B.S. and Ph.D. degrees in Convergence IT Engineering from Pohang University of Science and Technology, South Korea, in 2016 and 2022, respectively. From 2022 to 2024, she held a postdoctoral position in the Inter-University Semiconductor Research Center (ISRC) at Seoul National University, South Korea. She is currently an assistant professor in the Department of Semiconductor Systems Engineering at Sungkyunkwan University, South Korea. Her recent research explores AI-driven analog circuit design automation, including generative models for circuit topology generation. Her research also actively continues on the hardware-software co-design of efficient AI systems through neural network compression and deep learning accelerator design.

Abstract

Analog circuit design remains one of the most expertise-dependent areas in semiconductor engineering, with circuit topology design posing a particular bottleneck for automation. Recent advances in transformer-based models and large language models have sparked a new wave of research on AI-driven analog design, ranging from LLM-based topology refinement to fully generative device-level topology generation. In this talk, I will first review this rapidly evolving research landscape and discuss why existing approaches struggle with low electrical validity, memorization of training circuits, and reliance on human-in-the-loop training. I will then present AnalogToBi, a framework for device-level analog circuit topology generation that addresses these challenges through circuit-type conditioning, device renaming augmentation, a bi-partite graph circuit representation, and grammar-guided decoding. AnalogToBi generates electrically valid and structurally novel topologies without any human intervention during training, and SPICE-based case studies show that the generated circuits can be practically competitive. I will conclude by discussing future directions toward incorporating simulation feedback for performance-aware topology generation.

WiCAS SESSION

WiCAS 2

Chair: Sunghye Park (Ajou University, Korea)

14:10~14:40, MONDAY_OCTOBER 12, 2026

207 (2F)

Large Language Model Quantization: Foundations, Recent Advances, and Challenges

Seo Yeon Park

*Assistant Professor, Department of Computer Science & Engineering,
Hanyang University ERICA, Korea*



Biography

Seo Yeon Park is an Assistant Professor at Hanyang University ERICA. She received her Ph.D. in Computer Science from the University of Illinois Chicago and her M.S. in Computer Science from the University of Southern California. Previously, she worked as an AI/LLM Research Scientist Senior Manager at Accenture and an Applied Scientist Intern at Amazon Alexa NLU. Her research interests include natural language processing, information retrieval, and large language models.

Abstract

Quantization reduces the memory and computational costs of large language models (LLMs) by using lower-precision representations. This talk introduces the fundamentals of LLM quantization and reviews recent techniques for preserving accuracy, with a focus on handling activation outliers through rescaling and rotation. We conclude by discussing the limitations of existing approaches and ongoing research on mitigating massive outliers for more accurate and efficient low-bit inference.



OPENING CEREMONY

OPENING CEREMONY

MONDAY, OCTOBER 12

10:15~10:30 MONDAY, OCTOBER 12, 2026
Premier Ballroom (2F)

Welcome Address

Youngmin Kim

General Chair

(Hongik University, Korea)

Conference Statistics

Ilku Nam

Technical Program Committee Chair

(Pusan National University, Korea)

Announcements

Ilku Nam

Technical Program Committee Chair

(Pusan National University, Korea)

KEYNOTE SPEECHES

KEYNOTE SPEECHES

MONDAY, OCTOBER 12, 2026

Keynote Speech 1

10:30 ~ 11:20, MONDAY_OCTOBER 12, 2026

Premier Ballroom (2F)

Chair: Ilku Nam (Pusan National University, Korea)

SSD Controllers to AI Memory SoCs: Evolving SoC Architectures for Intelligent Memory Systems

Injae Koo

*VP & Head of SoC Design, SoC,
SK Hynix Solution Development, Korea*



Biography

Injae Koo is a Vice President at SK hynix, where he leads R&D and platform engineering for next-generation system-on-chip (SoC) solutions. His work centers on controller technologies for enterprise storage, mobile memory, and high-speed data movement—areas in which AI is redefining requirements for performance, energy efficiency, reliability, and security.

Injae Koo has led the development of storage-controller architectures from the SATA enterprise SSD era and PCIe Gen3 through PCIe Gen6. Before joining SK hynix in 2015, he held R&D and IC design roles at global semiconductor companies, working on storage controllers, 32-bit microcontrollers, and NAND flash systems.

Today, Koo is advancing scalable SoC platforms for next-generation enterprise SSDs, mobile memory controllers, and flash-buffer products, with a focus on chiplet integration and security-by-design.

KEYNOTE SPEECHES

Abstract

Two decades of System Innovation and the Road Ahead.

Over the past two decades, SSD controllers have been evolving from storage protocol engines into sophisticated system-on-chips integrating high-speed interfaces, embedded processors, cache management, NAND control, error correction code (ECC), security, power management, and workload-aware management.

This evolution has accelerated across successive PCIe generations. Each generation has introduced new architectural challenges beyond raw bandwidth, including massive parallelism, data movement, latency, power efficiency and hardware-software co-design. These challenges have driven innovations in cache architectures, specialized in-house processing, and increasingly intelligent control of storage resources.

The emergence of AI is now expanding this design space beyond conventional storage. AI systems require massive data movement across an increasingly heterogeneous system architecture spanning compute, memory, interconnect, and storage. As a result, the role of the SoC is evolving from controlling individual memory or storage devices toward orchestrating data across the broader memory system.

This keynote reflects on architectural lessons learned from more than two decades of SSD controller development, spanning multiple generations of client and enterprise PCIe SSDs. It then explores how these lessons can inform the next generation of AI memory SoCs and emerging memory solutions. Particular attention will be given to data movement, heterogeneous memory orchestration, domain-specific processing, energy efficiency and hardware-software co-design.

The central challenge ahead is no longer simply moving more data. It is enabling SoCs to move the right data, to the right compute resource, at the right time, with the right energy efficiency.

KEYNOTE SPEECHES

Keynote Speech 2

11:30~12:20, MONDAY_ OCTOBER 12, 2026

Premier Ballroom (2F)

Chair: Ilku Nam (Pusan National University, Korea)

The Physical AI Era: Building the Silicon for AI from Data Centers to the Edge and Using AI to Build the Silicon

Frank Schirrmeister

*Executive Director, Strategic Programs, Product & Markets Group,
System Verification and Validation, Synopsys, USA*



Biography

Frank Schirrmeister is Executive Director, Strategic Programs, System Solutions in Synopsys' Products & Markets Group. He leads strategic activities across system software and hardware assisted development for industries like automotive, data center and 5G/6G communications, as well as for horizontals like Artificial Intelligence / Machine Learning. Prior to Synopsys, Frank held various senior leadership positions at Arteris, Cadence Design Systems, Imperas, ChipVision, and SICAN Microelectronics, focusing on product marketing and management, solutions, strategic ecosystem partner initiatives, and customer engagement. He holds an MSEE from the Technical University of Berlin and actively participates in cross-industry initiatives as Panel Chair of the Design Automation Conference.

KEYNOTE SPEECHES

Abstract

Artificial intelligence is reshaping the semiconductor industry from two directions. On one side, AI has become the defining workload driving the development of next-generation silicon, from hyperscale data centers powering foundation model training and inference to edge and Physical AI systems such as autonomous vehicles, robotics, industrial automation, and intelligent devices. On the other side, AI is rapidly becoming an essential technology for designing, verifying, validating, and optimizing increasingly complex semiconductor systems. This dual transformation is defining the Physical AI Era. Drawing on examples from both cloud-scale and edge developments, this keynote explores the architectures emerging to support AI, including heterogeneous compute platforms, AI accelerators, advanced memory systems, chiplet-based designs, and tightly integrated hardware-software solutions.

As system complexity continues to outpace traditional engineering methodologies, verification, validation, software integration, and system optimization are becoming critical bottlenecks. AI is increasingly being applied throughout the engineering lifecycle, accelerating design exploration, test generation, debugging, software development, implementation, and system-level validation. We will discuss how semiconductor development is evolving toward AI-native workflows that combine simulation, emulation, prototyping, virtual platforms, and digital twins into a unified development continuum.

As AI expands from data centers to intelligent systems interacting with the physical world, success will depend not only on building the silicon that powers the next generation of AI, but also on reinventing how that silicon is conceived, designed, verified, and deployed. The organizations that master both transformations will define the future of the semiconductor industry.

KEYNOTE SPEECHES

KEYNOTE SPEECHES

TUESDAY, OCTOBER 13, 2026

Keynote Speech 3

10:10~11:00, TUESDAY_OCTOBER 13, 2026

Premier Ballroom (2F)

Chair: Yoko Uwate (Tokushima University, Japan)

Chip Design and Tape-out Courses including Agile-X, Agile Chip Design and Fabrication Platform for Updatable Chip Design

Makoto Ikeda

*Systems Design Lab. (d.lab), Engineering School,
The University of Tokyo, Japan*



Biography

Makoto Ikeda received B.E, M.E, and Ph.D. degrees all from Electronic Engineering, the University of Tokyo, in 1991, 1993, and 1996, respectively. He joined the University of Tokyo as a Research Associate in 1996, and is now a Full Professor, in Systems Design Lab.(d.lab), Engineering School, the University of Tokyo. He has been deeply engaged in the VLSI Design and Education Center (VDEC) activities, which is chip design platform for entire Japanese academia, from its foundation of 1996, and is now a director of d.lab, as well as a director of TSMC-Utokyo Lab, and a special advisor to the President of the University of Tokyo. He served as a Science Advisor to the Ministry of Education in 2024 and 2025. He served numerous positions in numerous conferences, including ISSCC 2021 ITPC Chair, VLSI Circuits Symposium 2019/17 Symp. And TPC Chairs, A-SSCC 2015 TPC Chair, and ASP-DAC 2027 General Chair. He is now a Society Vice-President of IEEE Solid-State Circuits Society, and President-Elect of IEICE, Engineering Sciences Society. He is a Senior member of IEEE and Fellow of IEICE.

KEYNOTE SPEECHES

Abstract

Japanese Ministry of Education(MEXT) has initiated a 10-year project named X-nics, in 2022, and selected 3 universities as the hub site, one of which is the University of Tokyo, in a title of "Agile-X: Democratizing platform for innovative semiconductor technology."

We have established Agile-X chip fabrication platform, which enables chip fabrication in 30-minute for the best case.

This talk will cover the basic concept, current achievement, and future perspectives of Agile-X platform.

This talk will introduce Agile-X chip design and fabrication platform, along with our long standing chip design and fabrication exercise courses in Department of EECE, the University of Tokyo.

KEYNOTE SPEECHES

Keynote Speech 4

11:10~12:00, TUESDAY_ OCTOBER 13, 2026

Premier Ballroom (2F)

Chair: Hoyoung Yoo (Chungnam National University, Korea)

Implementing Physical AI: Advanced Packaging and Agentic Design Automation

Yun Heo

*Product Engineering Director, ICD PE,
Cadence Design Systems, Korea*



Biography

Yun Heo is a Product Engineering Director at Cadence, where he leads technical support for 3D-IC design and agentic AI-based design solutions for customers in Korea. Previously, he worked in Samsung Electronics' System LSI Business, first designing Exynos mobile CPUs and later leading the development of RTL-to-GDS design methodologies in the Design Technology Team until 2022.

He received his B.S. and M.S. degrees in Electrical and Electronic Engineering from Yonsei University in 1999 and 2001, respectively, and his Ph.D. in Electrical and Computer Engineering from the University of Illinois at Urbana-Champaign in 2015.

KEYNOTE SPEECHES

Abstract

Physical AI brings perception, reasoning, and action into a continuous interaction with the physical world. For the chips powering these systems, implementation must deliver more than high AI throughput: critical sensing and control paths must remain responsive as inference workloads, memory traffic, power demand, and temperature change.

This keynote explores the implementation challenges of Physical AI through an advanced packaging architecture that integrates AI compute, control, I/O, and memory across multiple dies. It examines how workload dependencies and response-time requirements influence die partitioning, floorplanning, interconnect design, power delivery, and thermal management. Particular attention is given to the coupling between physical design decisions and sustained system behavior, where a change that improves bandwidth or compute density may also increase thermal coupling, power noise, or communication latency.

The keynote then presents a practical role for agentic AI in managing these interdependencies. By coordinating implementation and analysis tools, agents can translate operating scenarios into analysis plans, explore design alternatives, trace the impact of changes, and guide iterative optimization across signal integrity, power integrity, thermal, and timing constraints. Established solvers and explicit engineering requirements remain the basis for validation.

The central opportunity is a design flow that connects workload intent to verified physical implementation, helping engineers develop systems that meet performance and response-time requirements within realistic power, thermal, and reliability limits.

ORAL SESSIONS, Oct. 12

ORAL SESSIONS

MONDAY, OCTOBER 12

Samsung Electronics Session

MLAI 1

LLM Acceleration and Efficient Transformer Inference

Chair: Jaeha Kung (Korea University, Korea)

13:40~14:55, MONDAY _ OCTOBER 12, 2026
201+202 (2F)

MLAI1-1 (210)

CASE: Extending Composable Integer Arithmetic to Block-Scaled LLM Formats

13:40-13:55

Jaehyeck Choi and Jung-rae Kim
Sungkyunkwan University, Korea

MLAI1-2 (111)

Quantized Segmax with LoRA Compensation for Long-Context LLM Inference

13:55-14:10

Yongmin Park and Chae Eun Rhee
Hanyang University, Korea

MLAI1-3 (21)

DM-PIM: Repurposing DRAM Dummy Mats for Tall and Skinny GEMM Acceleration in Edge LLM Inference

14:10-14:25

Byungkuk Yoon and Jae-Joon Kim
Seoul National University, Korea

MLAI1-4 (10)

FAGE: An FPGA Accelerator for High-Throughput Graphormer Encode Processing

14:25-14:40

Min-Gwon Song, Min-Young Lee, Soomin Rho, Bohyeon Kang, and Ki-Seok Chung
Hanyang University, Korea

MLAI1-5 (151)

A Low-Complexity Min-p Token Sampler for Large Language Models

14:40-14:55

Yong-Gi Jo and Tae-Hwan Kim
Korea Aerospace University, Korea

ORAL SESSIONS, Oct. 12

ETRI Session

SoC 1

AI-Driven EDA and Design Optimization

Chair: Kon-Woo Kwon (Hongik University, Korea)

**13:40~14:40, MONDAY_ OCTOBER 12, 2026
204 (2F)**

SoC1-1 (92)

PRISM: Beam-Search Technology Mapping via Learned Physical Timing

13:40-13:55

Linyu Zhu¹, Xinyue Wu¹, Fan Hu¹, Li Li¹, Qing He², Yu He³, and Xinfei Guo¹

¹Shanghai Jiao Tong University, China

²Tongji University, China

³Hangzhou Phlexing Technology Co., Ltd, China

SoC1-2 (176)

LLM-Guided Initialization for Low-Budget Bayesian Optimization of FFT Hardware Designs

13:55-14:10

Nayoung Jung and Woo-Seok Choi

Seoul National University, Korea

SoC1-3 (25)

CABO: Circuit-Aware Bayesian Optimization for Efficient Analog Circuit Sizing

14:10-14:25

Jaehyung Jung, Seoyong Lee, and Kyumyung Choi

Sungkyunkwan University, Korea

SoC1-4 (186)

A Two-Stage Hybrid Framework for SAT Solver Runtime Prediction

14:25-14:40

Haimin Yan¹, Rui Ma¹, Tomohisa Kawakami², Tomoyasu Shimada¹, Xiangbo Kong³, Hiroyuki Tomiyama¹, and Shigeru Yamashita¹

¹Ritsumeikan University, Japan

²Duke University, USA

³Toyama Prefectural University, Japan

ORAL SESSIONS, Oct. 12

Synopsys Session

DCAS 1 Arithmetic and Computing Architectures

*Chair: Ambika Prasad Shah (Indian Institute of Technology Jammu, India)
Hyun Kim (Seoul National University of Science and Technology, Korea)*

13:40~14:55, MONDAY_ OCTOBER 12, 2026
205 (2F)

DCAS1-1 (20) Reconfigurable FP/INT×INT GEMM Accelerator With a Unified MXU

13:40-13:55 Jaeyong Jang, Jihoon Park, and Jae-Joon Kim
Seoul National University, Korea

DCAS1-2 (110) A Unified NTT/INTT Accelerator utilizing an MDC-based Memory Block for ML-KEM

13:55-14:10 Yeongo Kim, Taejun Park, and Youngmin Kim
Hongik University, Korea

DCAS1-3 (139) Scalable and Configurable Polynomial Arithmetic Architecture for Lattice-based PQC Schemes

14:10-14:25 Giseop Ahn, Quang Dang Truong, Yunseong Jang, and Hanho Lee
Inha University, Korea

DCAS1-4(240) A Feedback-Based Division-Free Iterative Normalizer for Stochastic Computing

14:25-14:40 Kitae Son, Jiho Kim, and Youngmin Kim
Hongik University, Korea

ORAL SESSIONS, Oct. 12

KETI Session

AC 1 Power Management Circuits

*Chair: Haruo Kobayashi (Gunma University, Japan)
Junwon Jeong (Sookmyung Women's University, Korea)*

**13:40~14:25, MONDAY_ OCTOBER 12, 2026
206 (2F)**

AC1-1 (47)

A SAR-Based Adaptive ZCD For Energy-Harvesting Buck-Boost Converter

13:40-13:55

Jung-Jin Choi, Ju-Won Oh, and Kang-Yoon Lee
Sungkyunkwan University, Korea

AC1-2 (222)

A 99.8% Tracking Efficiency Piezoelectric Energy Harvesting Circuit with Fast-MPPT Control

13:55-14:10

Tzung-Je Lee and Teng-Tai Sun
National Sun Yat-Sen University, Taiwan

AC1-3 (173)

A Recycling-Free Buck-Based SIBO Converter with Minimum Inductor Current for MicroLED Displays

14:10-14:25

Seungeon Lee and Kunhee Cho
Sungkyunkwan University, Korea

ORAL SESSIONS, Oct. 12

TeleChips Session

MLAI 2 AI Accelerator Architectures and FPGA Implementations

Chair: Youngjoo Lee (Korea Advanced Institute of Science & Technology, Korea)

15:10 ~ 16:25, MONDAY_ OCTOBER 12, 2026

201+202 (2F)

MLAI2-1 (179) **A Low-Latency and Energy-Efficient FPGA Accelerator for Hybrid Convolution-Transformer U-Net in Medical Image Segmentation**

15:10-15:25

Xingan Sha, Zeyuan Song, Senyu Lin, Jiaqi Lai, and Youhua Shi
Waseda University, Japan

MLAI2-2 (5) **Multi-Operating-Point Lightweight Super-Resolution via Sobel-Guided Early Exit and Channel Pruning**

15:25-15:40

Soyeon Ahn¹, Sukho Lee², and Moon Gi Kang¹
¹*Yonsei University, Korea*
²*Dongseo University, Korea*

MLAI2-3 (200) **Energy-Efficient Visual Inspection with FFT-Based CNNs and Adaptive Floating-Point Quantization**

15:40-15:55

Lukas Krupp¹, Marco Groß^{1,2}, Michael Graichen², Kim Ulrich², and Norbert Wehn¹
¹*University of Kaiserslautern-Landau (RPTU), Germany*
²*Wipotec GmbH, Germany*

MLAI2-4 (103) **Resource-Efficient BERT Accelerator with Activation-Based Structured Pruning**

15:55-16:10

Ping-Yu Hsieh, Ching-Te Chiu, and Yao-Wei Tang
National Tsing Hua University, Taiwan

MLAI2-5 (147) **An Area-Time-Efficient Pipelined Design for Binary Neural Networks**

16:10-16:25

Joseph Yousry Attalla, Patriot Benton, Tomas Aparicio, and Tuy Tan Nguyen
Florida State University, USA

ORAL SESSIONS, Oct. 12

TechwidU Session

SoC 2

Physical Design, Thermal, and Manufacturing Methodologies

Chair: Jiun-Lang Huang (National Taiwan University, Taiwan)

Changho Han (Kumoh National Institute of Technology, Korea)

15:10 ~ 16:10, MONDAY_ OCTOBER 12, 2026

204 (2F)

SoC2-1 (37)

Differentiable Thermal Proxies for Face-to-Face 3D Placement with PINN Audit

15:10-15:25

Xiao Wang, Yan Huo, Hai-Liang Li, Miao-Hui Hao, Xu Yang, and Bei-Ping Yan

Hong Kong Applied Science and Technology Research Institute (ASTRI), China

SoC2-2 (69)

A Thermal Via Pillar Insertion Methodology for Design Time Mitigation of BSPDN Thermal Penalty

15:25-15:40

M. Stassar^{1,2,3}, X. Chang¹, O. Zografos¹, C. Avdikou¹, M. Lofrano¹, J. Y. Lin¹, J. Myers¹, D. Milojevic^{1,3}, M. Naeim², and W. Chow²

¹IMEC, Belgium

²Cadence Design Systems, USA

³Université Libre de Bruxelles, Belgium

SoC2-3 (81)

Core-Halo ILT: A Modular Open-Source Framework for Full-Chip Mask Optimization

15:40-15:55

Young-Han Son¹, Deok-Joong Lee¹, Hyeonyeong Nam¹, Dong-Hee Shin², and Tae-Eui Kam¹

¹Korea University, Korea

²Yonsei University, Korea

SoC2-4 (39)

Generation of a Selective Grid-Based I/O-CPM for High-Speed Memory Interface Verification

15:55-16:10

Jiyong Cha^{1,2} and Eui-Young Chung¹

¹Yonsei University, Korea

²SK hynix Inc., Korea

ORAL SESSIONS, Oct. 12

Cadence Session

DCAS 2 Communication and Signal Processing Systems

Chair: Kyuho Lee (Yonsei University, Korea)

15:10 ~ 16:25, MONDAY_ OCTOBER 12, 2026
205 (2F)

DCAS2-1 (16) A Fully Standard-Cell-Flow Compatible DCO in 12 nm FinFET technology for BB-PLL applications

15:10-15:25

Marco Mestice, Furkan Aktas, Jan Lappas, Christian Weis, and Norbert Wehn
University of Kaiserslautern-Landau, Germany

DCAS2-2 (144) A High-Precision mUVT-Based Hopping DFT Architecture for FPGA Acceleration

15:25-15:40

Wen-Ho Juang, Chieh-Sen Chuang, and Zhi-Ning Yang
National Formosa University, Taiwan

DCAS2-3 (148) History-Related Stride Bank Predictor Architecture

15:40-15:55

Ipek Gecin¹, Taarun Jain¹, Emil Matus¹, and Gerhard Fettweis^{1,2}
¹*Technische Universität Dresden, Germany*
²*Barkhausen Institut, Germany*

DCAS2-4 (216) Hardware-level Complexity Analysis of Bistatic OFDM-Based ISAC Receiver

15:55-16:10

Junhyuk Park and Dongyun Kam
Ulsan National Institute of Science and Technology, Korea

DCAS2-5 (241) A Power-Gated Floating-Point FFT with FP32/FP16 Switching for Keyword Spotting in 180 nm CMOS

16:10-16:25

Akash Chinni, Dr. Shashidhar Tantry, Dhanashree G. Bhate
PES University, India

ORAL SESSIONS, Oct. 13

ORAL SESSIONS

TUESDAY, OCTOBER 13



MLAI 3

Edge AI Applications and Efficient Vision Systems

Chair: Won-Young Lee (Seoul National University of Science and Technology, Korea)

09:00 ~ 09:45, TUESDAY_ OCTOBER 13, 2026
201+202 (2F)

MLAI3-1(122)

09:00-09:15

An ISP-Free RAW Bayer Spiking U-Net Accelerator for Edge-SoC Semantic Segmentation

Yongbo Lin¹, Jiasheng Li¹, Huaxu Zhao¹, Jinfu Zhang¹, Dianyu Qi^{1,2}, and Yitao Ma^{1,2}

¹Zhejiang University, China

²ZJU-Hangzhou Global Scientific and Technological Innovation Center, China

MLAI3-2 (112)

09:15-09:30

Display-Plane Relation Distillation for Lightweight Multifocal Display Decomposition

Junseo Choi and Chae Eun Rhee

Hanyang University, Korea

MLAI3-3 (83)

09:30-09:45

ECG Heartbeat Classification Using Multi-Scale Dilated Convolution and Dynamic Spectral-Guided Gating

Shin-Chi Lai¹, Yao-Feng Liang¹, and Szu-Ting Wang²

¹National Formosa University, Taiwan

²Chaoyang University of Technology, Taiwan

ORAL SESSIONS, Oct. 13

AC/WL

Integrated Circuits for Next-Generation Communication and Energy-Efficient Systems

*Chair: Shin-Chi Lai (National Formosa University, Taiwan)
Jaeho Im (Hongik University, Korea)*

**09:00~10:00, TUESDAY _ OCTOBER 13, 2026
204 (2F)**

AC/WL-1 (182)

A PAM-4 Receiver with Time-Domain 2-Tap FIR and 1-Tap IIR DFE

09:00-09:15

Kiho Seong¹, Junsen He², Kwang-Hyun Baek³, and Tony Tae-Hyoung Kim¹

¹Nanyang Technological University, Singapore

²Micron Technology, USA

³Chung-Ang University, Korea

AC/WL-2 (60)

A 25-Gb/s Single-Ended PAM-4 Transceiver With Amplitude-Tunable Crosstalk Cancellation for On-Silicon Interconnection

09:15-09:30

Hanbin Jo, Seung-Beom Kim, Minwook Kim, and Seon-Kyoo Lee

Pohang University of Science and Technology, Korea

AC/WL-3 (207)

A Multi-Level LED Driver for VLC System Achieving 99.3% Settling in 1.25τ

09:30-09:45

Sin-Won Kim, Woon-Ho Kim, and Dong-Woo Jee

Ajou University, Korea

AC/WL-4 (14)

A 40-Gb/s NRZ Mixed-Signal Receiver With Sampling-Based Equalization in 28-nm CMOS

09:45-10:00

Keebong Hyun¹, Donghyeon Kim¹, Woo-Young Choi¹, and Tae-Young Choi²

¹Yonsei University, Korea

²Cadence, Korea

ORAL SESSIONS, Oct. 13

ET 1

Emerging Technologies for Advanced Computing

Chair: Tzung-Je Lee (National Sun Yat-Sen University, Taiwan)

09:00~10:00, TUESDAY_ OCTOBER 13, 2026
205 (2F)

ET1-1 (3)

09:00-09:15

A 22-nm Embedded STT-MRAM with Fast 5ns Read Access Time and 0.54V Low-Power Operation

A. Antonyan¹, V. Kumar², S. Kumar², B. Prickett¹, P. Pandey², D. Nguyen³, R. Sharma², D. Chakraborty², H. Harshul², A. Dang³, Hai T. N. Tran³, P. T. Minh³, N. L. Tri³, T. H. Le³, L. Vo³, and H. Vu³

¹Synopsys, Sunnyvale, USA

²Synopsys, Noida, India

³Synopsys, Ho-Chi-Minh, Vietnam

ET1-2 (51)

09:15-09:30

Back-Pattern Dependency Minimization Techniques to Improve Accuracy of NAND Flash-based PIM

Hyunjin Kim and Jae-Joon Kim
Seoul National University, Korea

ET1-3 (79)

09:30-09:45

Verification of Phase Area Analysis Beacon-based Spy-camera Prevention System

Koki Soboi¹, Takeshi Kumaki², and Kyosuke Kageyama¹

¹Kindai University, Japan

²Ritsumeikan University, Japan

ET1-4 (174)

09:45-10:00

A Measurement-Aware Forward-Inverse Jointly Trained TNN Framework for PSP103.2 Parameter Extraction

Yewon Kim¹, Hyunyoung Yoo¹, Jeongtaek Kim¹, Seuk Jung¹, Taeho Jung¹, Jusung Kim², and Jae-Won Nam¹

¹Seoul National University of Science and Technology, Korea

²Ewha Womans University, Korea

ORAL SESSIONS, Oct. 13

AC 2

Analog Techniques

Chair: Seong-Jin Kim (Sogang University, Korea)

**09:00~10:00, TUESDAY_ OCTOBER 13, 2026
206 (2F)**

AC2-1 (293)

09:00-09:15

A High-Dynamic-Range, High-Gain, Wideband, Low-Noise Transimpedance Amplifier

K. Ashoka Deepthi and Arup Polley
Indian Institute of Science, India

AC2-2 (4)

09:15-09:30

A Curvature-Compensated Bandgap Reference with Decoupled PTAT/CTAT Generation and Low Temperature Drift Correction

Lubin Xiang, Zhihao Li, Xiaobo Gong, Ming Zhu, Qiang Zhao, Zhigang Li, and Chunyu Peng
Anhui University, China

AC2-3 (136)

09:30-09:45

A 4.837 ppm/°C Curvature-Compensated Bandgap Reference With Digital Auto-Calibration and $\pm 0.067\%$ 3σ Inaccuracy

Yi Zeng, Zhenhao Fan, Zili Zhou, and Menglian Zhao
Zhejiang University, China

AC2-4 (211)

09:45-10:00

A Fully Integrated Energy Harvesting PMIC with Kickback-Immune LDO for Battery-Less IoT

Sung-Gyu Kim^{1,2}, Ju-Won Oh^{1,2}, and Kang-Yoon Lee^{1,2}
¹*Sungkyunkwan University, Korea*
²*SKAIChips, Korea*

ORAL SESSIONS, Oct. 13

RF 1

Advanced Frequency Generation and Synthesis Circuits

Chair: Jeongwhan Han (Chungnam National University, Korea)

**09:00~10:00, TUESDAY_ OCTOBER 13, 2026
207 (2F)**

RF1-1 (7)

09:00-09:15

An X-Band Sub-Sampling PLL Featuring a TDCBased Lock Detector for Robust Switching Control

Chun-Yi Chiang, Jyun-Yan Lin, Wei-Chen Chung, and Yue-Fang Kuo
Yuan Ze University, Taiwan

RF1-2 (137)

09:15-09:30

A Second-Order Approximation-Based Calibration Technique for QDAC-Based Two-Point Modulation PLL

Tae-seok Song, Jun-kyo Park, and Byung-sung Kim
Sungkyunkwan University, Korea

RF1-3 (26)

09:30-09:45

A Wideband Dual-Band Voltage-controlled Oscillator Using a Reconfigurable Current-Folding Frequency Multiplier with a Bias-Controlled Varactor-Tuned BPF

Yu-Qiao Hsu, Ruei-Wen Li, Yong-Jie Lee, and Yue-Fang Kuo
Yuan Ze University, Taiwan

RF1-4 (133)

09:45-10:00

A 60-GHz Low-Phase-Noise Dual-Core Class-F Push-Push VCO in 28-nm FD-SOI

Jae-Hyo Shin, Tae-Jeong Kim, Jun-Kyo Park, and Byung-Sung Kim
Sungkyunkwan University, Korea

ORAL SESSIONS, Oct. 13

Samsung Electronics Session

DC 1 High-Speed and High-Resolution Data Converters

Chair: Young-Ha Hwang (Soongsil University, Korea)

13:20~14:35, TUESDAY_ OCTOBER 13, 2026

201+202 (2F)

DC1-1 (117) A Continuous-Time Zoom ADC with a Negative-R Residue-Amplifying Inter-stage Filter

13:20-13:35

Seokho Yoon¹, Suyoung Chon¹, Junghyun Yoon¹, and Youngcheol Chae^{1,2}

¹Yonsei University, Korea

²XO Semiconductor Inc., Korea

DC1-2 (128) An 8-Bit 1-GS/s 23.1-fJ/Conv.-Step Asynchronous 2b/Cycle SAR ADC With Time-Domain Quantization

13:35-13:50

Donghyeok Kim and Young-Ha Hwang

Soongsil University, Korea

DC1-3 (73) A 6-bit 1.75GS/s SAR ADC with Ping-Pong Comparator and Hybrid Offset Calibration

13:50-14:05

Jie-Da Cai, Chu-Yu Ou-Yang, and Hsin-Shu Chen

National Taiwan University, Taiwan

DC1-4 (291) A 12-Bit Arbitrary Waveform Generator for Microelectrode-Array Electrochemical Analysis

14:05-14:20

Ji-Min Oh and Young-Ha Hwang

Soongsil University, Korea

DC1-5 (196) An 8-bit 10-GS/s Time-Interleaved SAR ADC for Short-range Wireless Links

14:20-14:35

Hyeon-Gi Hwang and Dong-Ryeol Oh

Jeju National University, Korea

ORAL SESSIONS, Oct. 13

Synopsys Session

SoC 3

Hardware Security, Test, and Reliability

Chair: Hoyoung Yoo (Chungnam National University, Korea)

13:20~14:35, TUESDAY_ OCTOBER 13, 2026
204 (2F)

SoC3-1 (205)

SAGE: Sparse Anonymous Grouping and Extraction for AES Subround Leakage

13:20-13:35

Jincheol Jeong and Hoyoung Lee
Ajou University, Korea

SoC3-2 (150)

Multi-Variate Higher-Order Side-Channel Leakage Assessment with Deep Learning Dimensionality Reduction

13:35-13:50

Ku-Ting Chou and Jiun-Lang Huang
National Taiwan University, Taiwan

SoC3-3 (194)

Measuring Information Ceilings in Scan-Chain Diagnosis

13:50-14:05

Yunsik Kim and Hoyoung Lee
Ajou University, Korea

SoC3-4 (30)

High-speed Address Generator Utilizing Ring-based Architecture for Memory Testing

14:05-14:20

Duyeon Won, Juyong Lee, Seung Ho Shin, Gyeonggyu Park, and Sungho Kang
Yonsei University, Korea

SoC3-5 (219)

A Unified Open Radiation SPICE Framework for 28 nm Bulk, FDSOI, and PD-SOI SoC Benchmarks

14:20-14:35

Qing Zhang^{1,2}, Chao Wang², and Yongfu Li²
¹*Shenzhen University, China*
²*Shanghai Jiao Tong University, China*

ORAL SESSIONS, Oct. 13

ETRI Session

ET 2

Circuits & Systems for Emerging Applications

Chair: Yongtae Kim (Kyungpook National University, Korea)

13:20~14:35, TUESDAY_ OCTOBER 13, 2026

205 (2F)

ET2-2 (70)

13:35-13:50

Thermal-Aware Power Integrity Optimization of PVSS Return Paths in 2.5D Glass Interposer PDNs

Jaeyoung Choi¹, SeungJin Lee¹, Suin Chae^{1,2}, Hyunseuk Ahn², Jung Han Choi³, Jin Yu², and Jaemyung Lim¹

¹*Hanyang University, Korea*

²*Korea Electronics Technology Institute, Korea*

³*Fraunhofer Institute for Telecommunications Heinrich-Hertz-Institut, Germany*

ET2-3 (80)

13:50-14:05

Evaluation of Weighted-ZCR Slope for Animal Ear-like Hazardous Sound Detection Device

Futa Goto¹, Yuki Muikaichi¹, Takeshi Kumaki², and Kyosuke Kageyama¹

¹*Kindai University, Japan*

²*Ritsumeikan University, Japan*

ET2-4 (42)

14:05-14:20

5T-SRAM Cell using Reconfigurable Field-Effect Transistors

Julian Kulenkampff, Viktor Weinelt-Choi, and Klaus Hofmann

Technical University of Darmstadt, Germany

ET2-5 (140)

14:20-14:35

Pair-Mapping-Aware De-Embedding for Low-Overhead IR Drop Compensation in RRAM Compute-in-Memory Accelerators

Hanhee Jung and Woo-Seok Choi

Seoul National University, Korea

ORAL SESSIONS, Oct. 13

Openedges Technology Session

RF 2

RF Front-end Circuits and Wireless Systems

Chair: *Szu-Ting Wang (Chaoyang University of Technology, Taiwan)*
Jusung Kim (Ewha Womans University, Korea)

13:20~14:35, TUESDAY_ OCTOBER 13, 2026
206 (2F)

RF2-1 (28)

13:20-13:35

A Mixer-First Receiver Front-End Achieving 3× Passive Voltage Gain and Robust Harmonic Suppression Using a Six-Phase Clock

Xinyi Chu, Youming Zhang, Xusheng Tang, and Fengyi Huang
Southeast University, China

RF2-2 (201)

13:35-13:50

A Blocker-Tolerant Wideband Receiver Employing a Frequency-Selective Positive- and Negative-Capacitive-Feedback TIA for Drone Detection

Back Lee, Jungseob Lim, Siwoong Park, and Donggu Im
Jeonbuk National University, Korea

RF2-3 (95)

13:50-14:05

A 2.4GHz Ultra-Low Power Mixer First Internet of Things Receiver Front-End

Kobina Ankomah Addison¹, Seunghyun Cho², and Jusung Kim²
¹*Hanbat National University, Korea*
²*Ewha Womans University, Korea*

RF2-4 (12)

14:05-14:20

5G FR3 Band Watt-Level Broadband Stacked PA Design in 40 nm GaN HEMT

Omar Elgarhy¹, Clint Sweeney¹, Donald Y.C. Lie¹, and Jerry Lopez^{1,2}
¹*Texas Tech University, USA*
²*NoiseFigure Research, Inc., USA*

RF2-5 (198)

14:20-14:35

A Compact Current Mode Analog Baseband Employing an Inverter-Based Transimpedance Low-Pass Filter for IR-UWB Receivers

Mingyu Park, Chansoo Park, and Minyoung Song
Daegu Gyeongbuk Institute of Science and Technology, Korea

ORAL SESSIONS, Oct. 13

ASICLAND Session

MLAI 4

Efficient AI Computing: Quantization, Pruning, and Neuro-morphic Computing

Chair: Dongyun Kam (Ulsan National Institute of Science and Technology, Korea)

14:50~16:05, TUESDAY_ OCTOBER 13, 2026

201+202 (2F)

MLAI4-1 (109)

14:50-15:05

Fisher Information Guided Mixed-Precision Quantization for Microscaling Formats

Taejun Park and Youngmin Kim
Hongik University, Korea

MLAI4-2 (119)

15:05-15:20

A Layer-Wise Design-Space Exploration Framework for Heterogeneous SRAM/RRAM Compute-in-Memory Architectures

Jiwon Yoo and Woo-Seok Choi
Seoul National University, Korea

MLAI4-3 (98)

15:20-15:35

SASMT: A Spike-Based Adaptive Structured Mask Pruning Algorithm for Transformers

Nai-Jen Sung¹, Pin-Yue Wang¹, Yun-Chung Lin¹, Chih-Cheng Lu², and Kea-Tiong Tang¹
¹*National Tsing Hua University, Taiwan*
²*Industrial Technology Research Institute, Taiwan*

MLAI4-4 (204)

15:35-15:50

Spiking Actor-Critic for Quadruped Locomotion: Spike Encoding Schemes Compared

Volkan Un, Juan A. Cabrera, and Frank H. P. Fitzek
Technische Universität Dresden, Germany

MLAI4-5 (50)

15:50-16:05

Scaling Logic Gate Networks with ConvLogicMixer

Lukas Korinek and Jaeha Kung
Korea University, Korea

ORAL SESSIONS, Oct. 13

SIEMENS Session

WL

Advanced Wireline Transceivers and Clocking Techniques

Chair: Junyoung Song (Incheon National University, Korea)

14:50~16:05, TUESDAY_ OCTOBER 13, 2026

204 (2F)

WL-1 (197)

14:50-15:05

A 36Gb/s 0.104pJ/bit Dual-Threshold Receiver for Relaxing the Feedback Timing Constraint

Gyuwon Jeon, Jongchan An, Seung-Myeong Yu, Myeongju Park, Mingyun Kim, Gwangmyeong An, Songi Cheon, and Junyoung Song

Incheon National University, Korea

WL-2 (155)

15:05-15:20

A 30-Gb/s/pin Single-Ended PAM-3 Transmitter With a Capacitor-Less Hybrid Pre-Emphasis FFE

Jihyeok Lee and Young-Ha Hwang

Soongsil University, Korea

WL-3 (48)

15:20-15:35

A 16-GHz Multi-phase Clock Generator with Input-Swapped QPD Reuse for Path-Mismatch Calibration

Daehoon Na^{1,2}, Kahyun Kim¹, and Woo-Seok Choi¹

¹*Seoul National University, Korea*

²*Samsung Electronics, Korea*

WL-4 (206)

15:35-15:50

A 40Gb/s 0.402pJ/b PAM-4 Receiver Using a Self-Referenced LSB Comparator

Myeongju Park, Gyuwon Jeon, Jongchan An, Mingyun Kim, Yeoncheol Noh, and Junyoung Song

Incheon National University, Korea

WL-5 (61)

15:50-16:05

A 40-Gb/s 0.6-VDDQ Single-Ended PAM-4 LVSTL Transmitter With FFE and In-Lane DBI for Low-Power Memory Interfaces

Han-UI Song, Sunghoon Kim, Hanmin Choi, and Seon-Kyoo Lee

Pohang University of Science and Technology, Korea

ORAL SESSIONS, Oct. 13

DCAS 3

Memory and In-Memory Computing Systems

Chair: Hoyoung Yoo (Chungnam National University, Korea)

14:50~16:05, TUESDAY_ OCTOBER 13, 2026
205 (2F)

DCAS3-1 (13)

Bank-Group and Read-Pressure Integrated Drain Scheduling with Guarded Exit

14:50-15:05 Jaebin Eom and Eui-Young Chung
Yonsei University, Korea

DCAS3-2 (62)

SPARS-11T: A Side-Channel Power Analysis Attack Resilient Secure SRAM Design

15:05-15:20 Umayia Mushtaq , Sandeep Kour , and Ambika Prasad Shah
Indian Institute of Technology Jammu, India

DCAS3-3 (72)

Error-Recoverable Approximate BF16 Digital CIM

15:20-15:35 Yuhyeon Jin and Munhyeon Kim
Seoul National University, Korea

DCAS3-4 (138)

A 1-kb 1T1C HZO FeRAM Design With Robust Sensing and Automatic Write-Back Control

15:35-15:50 Ya-Chuan Chang¹, Yi-Chun Lin¹, L S S Pavan Kumar Chodiseti¹,
Leenendra Chowdary Gunnam^{1,2}, and Chua-Chin Wang¹
¹*National Sun Yat-sen University, Taiwan*
²*SRM University-AP, India*

DCAS3-5 (209)

Configurable Mismatch-Tolerant Multi-Bit SRAM-based In-Memory Computing Architecture

15:50-16:05 Sandeep Kour and Ambika Prasad Shah
Indian Institute of Technology Jammu, India

SPECIAL SESSIONS, Oct. 12

SPECIAL SESSIONS

MONDAY, OCTOBER 12

SS 1

Korea-Japan Joint Session for Advanced IC Designs

Organizer: Prof. Jae-Yoon Sim (Pohang University of Science and Technology, Korea)

Abstract: The Institute of Electronics, Information and Communication Engineers (IEICE) has been the biggest institute in the areas of electrical engineering and associated fields in Japan. As one of the international collaborative activities between the IEICE and the Institute of Semiconductor Engineers (ISE) of Korea, this special session is organized to introduce research activities from the Electronic Society of IEICE and ISE in the areas of advance integrated circuit (IC) designs. It will give valuable time for exchanging technical ideas and sharing experiences on advanced topics of IC designs as well as opportunities of fruitful networking for possible international collaborations between researchers in Korea and Japan.

Chair: Prof. Jae-Yoon Sim (Pohang University of Science and Technology, Korea)

15:10~16:40, MONDAY_OCTOBER 12, 2026
206 (2F)

SPECIAL SESSIONS, Oct. 12

SS1-1 (300)

15:10-15:25

[Invited] Fast-Transient On-Chip LDOs Powering AI and HPC SoCs

Jun-Eun Park

Sungkyunkwan University, Korea

SS1-2 (299)

15:25-15:40

[Invited] Hierarchical Hardware for Physical AI: 3D-Stacked GPU-on-Memory and Low-Power Wired-Logic DNN Processors

Atsutake Kosuge

The University of Tokyo, Japan

SS1-3 (298)

15:40-15:55

[Invited] Physics-Inspired Unconventional Computing and Memory

Bongjin Kim

Korea Advanced Institute of Science and Technology, Korea

SS1-4 (303)

15:55-16:10

[Invited] Shuttling-Based Sparse Silicon Spin-Qubit Architecture for Quantum Error Correction

Takashi Takemoto, Satoru Akiyama, Ryo Nagai, Yusuke Kanno, Saki Tanaka, Ryouta Katsube, Tatsuya Tomaru, Noriyuki Lee, Takuma Kuno, Takeru Utsugi, Masaharu Kinoshita, Yusuke Wachi, Takayasu Norimatsu, Ryuji Ukai, Atsushi Miyamoto, Hideo Arimoto, Nobuhiro Kusuno, Goichi Ono, Digh Hisamoto, Ryuta Tsuchiya and Hiroyuki Mizuno

Hitachi, Ltd., Japan

SS1-5 (302)

16:10-16:25

[Invited] Advanced I/O Circuit Techniques for Next-Generation Memory Interfaces

Seon-kyoo Lee

Pohang University of Science and Technology, Korea

SS1-6 (304)

16:25-16:40

[Invited] Cryogenic Analog-to-Digital Converters for Scalable Spin Qubit Controllers

Ryozo Takahashi and Takuji Miki

Kobe University, Japan

SPECIAL SESSIONS, Oct. 12

SS 2

Design, Analysis and Tools for Integrated Circuits and Systems (DATICS)

Organizers: Prof. Ka-Lok Man (Xi'an Jiaotong-Liverpool University, China)

Abstract: DATICS workshops/special sessions were initially created by a network of researchers and engineers both from academia and industry in the areas of Design, Analysis and Tools for Integrated Circuits and Systems (DATICS). The proposed DATICS-ISOCC'26 special session will focus on emerging Circuits and Systems (CAS) topics that will strongly lead human life revolutions, especially in CMOS technologies, communication technologies and biomedical technologies. Human life revolutions come along with economic opportunities. The market for these emerging topics is also forecast to grow to a multi-billion dollar market in the coming decade. The special session will highlight the potential and current developments of these CAS topics, along with pressing challenges. The proposed session is coherent and complementary to the conference theme and areas of interest of ISOCC. The main target of DATICS-ISOCC'26 is to bring together engineering researchers and people from industry to exchange theories, ideas, techniques and experiences. In addition, DATICS Yearly Special Session has been carried out at ISOCC since 2012.

Chair: Ka-Lok Man (Xi'an Jiaotong-Liverpool University, China)

15:10~16:55, MONDAY_OCTOBER 12, 2026
207 (2F)

SPECIAL SESSIONS, Oct. 12

SS2-1 (15)	Design Considerations for TinyML-Assisted Phase Interferometry AoA Estimation
15:10-15:25	Antonello Florio ¹ , Stefano Lioce ^{1,2} , Ka Lok Man ³ , and Gianfranco Avitabile ¹ ¹ Politecnico di Bari, Italy ² Centre Inria d'Université Côte d'Azur, France ³ Xi'an Jiaotong-Liverpool University, China
SS2-2 (17)	Self-Mixing Phase Interferometry for Low-Complexity AoA Estimation in Hybrid RISs
15:25-15:40	Stefano Lioce ^{1,2} and Gianfranco Avitabile ² ¹ Centre Inria d'Université Côte d'Azur, France ² Politecnico di Bari, Italy
SS2-3 (18)	A 5-Level Supply-Boosted Bipolar Pulser for Ultrasound Medical Imaging
15:40-15:55	Marco Rossano and Gianfranco Avitabile Politecnico di Bari, Italy
SS2-4 (38)	More Secure Fibonacci Q-matrix based Encryptions/Decryptions using Out-of-Order Executions
15:55-16:10	Tso-Bing Juang and Huang-Sen Chiu National Pingtung University, Taiwan
SS2-5 (65)	Analysis and Design of a Triple-Layer Cavity-Backed Slot Antenna for Dual-Band Sub-6 GHz Applications
16:10-16:25	Ziyi Gao, Jingchen Wang, Zhao Wang, Jie Zhang, Rui Pei, Qian Dong, Ka Lok Man, and Eng Gee Lim Xi'an Jiaotong-Liverpool University, China
SS2-6 (180)	Reinforcement learning for robot movement optimization aided by proximal policy optimization
16:25-16:40	Shijian Huang, Tongjian Yu, Nanlin Jin, Ho-Pun Lam, and Ka Lok Man Xi'an Jiaotong-Liverpool University, China
SS2-7 (294)	OmniWeather-GS: Radar-Anchored 3D Gaussian Fields for All-Weather Road-side Perception
16:40-16:55	Yu Du ¹ , Ho-Pun Lam ¹ , Jeremy S. Smith ² , Ka Lok Man ¹ , and Yutao Yue ^{3,4} ¹ Xi'an Jiaotong-Liverpool University, China ² University of Liverpool, United Kingdom ³ The Hong Kong University of Science and Technology (Guangzhou), China ⁴ The Jiangsu Industrial Technology Research Institute, China

SPECIAL SESSIONS, Oct. 13**SPECIAL SESSIONS**
TUESDAY, OCTOBER 13**SS 3****Emerging techniques of computing-in-memory and neuromorphic**

Organizers: Prof. Kyeong-Sik Min (Kookmin University, Korea)

Abstract: The relentless growth of data-intensive AI workloads has exposed the fundamental limitations of conventional von Neumann architectures, where the physical separation of memory and processing units imposes severe energy and latency penalties—the so-called “memory wall.” Computing-in-memory (CIM) and neuromorphic systems have emerged as compelling paradigms to overcome this bottleneck by performing computation directly within or near the memory array, thereby drastically reducing data movement and improving energy efficiency. This special session brings together recent advances spanning device, circuit, and architecture levels. Topics include CIM macros based on SRAM, DRAM, and emerging non-volatile memories such as RRAM, MRAM, and FeRAM; analog and mixed-signal techniques for high-precision in-memory multiply-accumulate operations; and neuromorphic circuits that emulate biological spiking and learning behavior for energy-efficient edge intelligence. By uniting perspectives from emerging devices, analog circuit design, and system-level architecture, this session aims to provide attendees with a comprehensive view of the state of the art and to stimulate discussion on future research directions toward practical, manufacturable CIM and neuromorphic hardware.

Chair: Kyeong-Sik Min (Kookmin University, Korea)

13:20~14:20, TUESDAY _ OCTOBER 13, 2026
207 (2F)

SPECIAL SESSIONS, Oct. 13

SS3-1 (87)

13:20-13:35

A 55-nm 8-Mb NOR-Flash CIM SoC with Slide-and-Follow Sampling and End-to-End Face-Detection Deployment

Y. P. Hong, J. W. Nam, Y. S. Kim, S. Y. Lee, B. S. Kim, H. W. Kye, J. H. Kim, W. J. Moon, H. B. Kim, C. Lu, S. W. Moon, S. H. Moon, S. H. Kim, and C. H. Lee
Pebble Square Inc., Korea

SS3-2 (220)

13:35-13:50

Hardware-Software Co-Design of Partitioned Quantization and Selective KV Access for Long-Context LLM Inference

Jingke Wang, Yizhe Wang, and Liang Chang
University of Electronic Science and Technology of China, China

SS3-3 (292)

13:50-14:05

Ferroelectric-Based CIM Techniques for Low-Power Edge AI

Kyeong-Sik Min
Kookmin University, Korea

SS3-4 (296)

14:05-14:20

A Target-Modulated Learning Framework for Biologically Plausible and Efficient SNNs

Kalkidan Deme Muleta
Sungkyunkwan University, Korea

SPECIAL SESSIONS, Oct. 13

SS 4

Hardware and software design techniques for AI processing platforms

Organizers: Prof. Won-Young Lee (Seoul National University of Science and Technology, Korea)

Abstract: In recently years, artificial intelligence (AI) is known as the core driving force of the next industrial revolution, and its applications have been advanced in many fields such as computer vision, language understanding, auto-driving, and robotics. Since AI software has grown in complexity, demands on reliable and high performance computing systems consistently are growing. Therefore, the advanced hardware and software techniques beyond von Neumann computers have been studied for AI processing platform to execute AI algorithms at reasonable speed. In this special session, five papers will discuss emerging techniques for enhancements of AI processing platforms regarding AI algorithms, processing architectures, hardware implementations and software developments.

Chair: Won-Young Lee (Seoul National University of Science and Technology, Korea)

14:50~16:05, TUESDAY_ OCTOBER 13, 2026
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SPECIAL SESSIONS, Oct. 13

SS4-1 (11)

14:50-15:05

Analysis of Geometric Feature Limitations in Wafer Defect Pattern Recognition

Taehyeon Kim, Minho Choi, and Hwajung Kim

Seoul National University of Science and Technology, Korea

SS4-2 (67)

15:05-15:20

RLE-Aware Weight Loader: A Lightweight Decompression Front-End for Fast LLM Cold Starts

Jaeyoung Choi and Jaehyeong Sim

Ewha Womans University, Korea

SS4-3 (91)

15:20-15:35

ACIO Encoder: Always Complete Isolation of Outliers for Low-Precision LLM Quantization

Jihyeon Hwang, Jungwoo Park, Taehong Min, and Seung Eun Lee

Seoul National University of Science and Technology, Korea

SS4-4 (108)

15:35-15:50

Training-Free Layer-Reuse Self-Speculative Decoding for Lossless LLM Inference Acceleration

Jeongho Kim, Jihoon Jang, and Hyun Kim

Seoul National University of Science and Technology, Korea

SS4-5 (175)

15:50-16:05

FBFET-Based Parabolic Hysteresis-Emulated Chaotic Random Number Generation

Minyoung Kim¹, Yukyung Jeong¹, Hyunyoung Yoo¹, Dongjun Jang², Jaewon Lee¹,
Ganghyeon Park¹, Seungchan Lee¹, Min-Woo Kwon¹, and Jae-Won Nam¹

¹*Seoul National University of Science and Technology, Korea*

²*Sogang University, Korea*

SPECIAL SESSIONS, Oct. 13

SS 5

Circuits and Systems for AI, Security and Advanced Computing

Organizers: Prof. Hanho Lee (Inha University, Korea)

Abstract: This special session, Circuits and Systems for AI, Security and Advanced Computing explores cutting-edge solutions for power efficiency, signal precision, memory reliability, and emerging computing paradigms. It addresses these critical hardware challenges through six innovative papers divided into three key domains:

1. Power Management and Precision Interfaces

Presents a hybrid buck-boost DC-DC converter achieving over 54% inductor current reduction for Li-ion applications.

Introduces a multi-mode auto-zeroing incremental $\Delta\Sigma$ ADC that optimizes noise and amplifier settling in precision sensor interfaces.

2. Reliable Memory and AI Hardware

Proposes a reliability-driven redundancy analysis method for interleaved-ECC memory to maximize uncorrectable codeword reduction.

Showcases a dual-mode flash computing-in-memory (CIM) architecture enabling energy-adaptive, variation-tolerant AI inference.

3. Post-Quantum and Quantum Computing

Details noise-aware approximate quantum adder designs using relative-phase Toffoli gates to reduce quantum costs in NISQ environments.

Describes a unified, pipelined RM(1,7) decoder optimized for Hamming Quasi-Cyclic (HQC) post-quantum cryptography decapsulation.

Together, these presentations provide a comprehensive look at the advanced circuit and system-level techniques vital for building intelligent, secure, and resilient electronic systems.

Chair: Hanho Lee (Inha University, Korea)

14:50~16:20, TUESDAY_OCTOBER 13, 2026

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SPECIAL SESSIONS, Oct. 13

SS5-1 (33)

14:50-15:05

An Always-Dual-Path Hybrid Buck-Boost Converter Achieving 56% Inductor Current Reduction

Gyumin Kim, Junseong Hwang, Kieun Kim, and Inho Park
Inha University, Korea

SS5-2 (86)

15:05-15:20

A Dual-Mode Flash Computing-in-Memory Architecture for Energy-Adaptive AI Inference

Dayeon Yu, Hwiho Hwang, Jonghwan Yoo, and Hyungjin Kim
Hanyang University, Korea

SS5-3 (89)

15:20-15:35

A Unified RM(1,7) Decoder Architecture with Intra-Stage Pipelining for HQC

Muhammad Fajri Sachruddin, Muhammad Ogün Hasanuddin, and Hanho Lee
Inha University, Korea

SS5-4 (99)

15:35-15:50

Relative-Phase Toffoli Gate-Based Low-Cost Approximate Quantum Adders Design

Taegyun Kim and Yeongkyo Seo
Inha University, Korea

SS5-5 (102)

15:50-16:05

A 24-bit Multi-Mode AZ-Integrator-Based Incremental $\Delta\Sigma$ ADC for Precision Sensor Interfaces

Kangjae Lee, Donghwan Kim, and Jaehoon Jun
Inha University, Korea

SS5-6 (104)

16:05-16:20

Reliability-Driven Redundancy Analysis for Interleaved-ECC Memory Repair

Keonwoo Kim¹, Jin Hwan Park², Minsuk Sung³, and Young-woo Lee¹
¹*Inha University, Korea*
²*Teradyne Inc., USA*
³*Tanhay Inc., Korea*



POSTER SESSIONS, Oct. 13

POSTER SESSIONS

TUESDAY, OCTOBER 13



Poster Session

Chair: Ji-Hoon Kim (Hanyang University, Korea)

Standing Time 09:00~16:05, TUESDAY, OCTOBER 13, 2026
Exhibition Time 16:05~16:45, TUESDAY, OCTOBER 13, 2026
LOBBY (2F)

Analog Circuits

PS-1 (2)

Band-Selective Spread Spectrum Technique for EMI Reduction in SIDO DC-DC Converters

Yasunori Kobori¹, Yifei Sun², Guiyi Dong³, Nobukazu Tsukiji⁴, Ramin Khatami³
Takuya Arafune³, Shogo Katayama³, Anna Kuwana³, and Haruo Kobayashi³

¹*Maebashi Institute of Technology, Japan*

²*Shenyang University of Chemical Technology, China*

³*Gunma University, Japan*

⁴*National Institute of Technology (KOSEN), Gunma College, Japan*

PS-2 (52)

A Dual-Path Cold-Start with Adaptive Body Biasing for Wide-Input-Range Energy Harvesting Systems

Hye Ju Shin, Ju Won Oh, and Kang Yoon Lee
Sungkyunkwan University, Korea

PS-3 (116)

A 0.35-V, 384-pW CMOS Voltage Reference for -40 °C to 165 °C Operation

Hyung In Kim and Hongil Yoon
Yonsei University, Korea

POSTER SESSIONS, Oct. 13

PS-4 (145)

An 11-Bit 1.953-ps-Resolution, 4-ns-Range DTC with PI-Based Calibration for Radar Target Simulators

Gi-Heon Ryu and Byung-Sung Kim
Sungkyunkwan University, Korea

PS-5 (153)

Series Capacitor-based Low-power DCO for Wide Tuning Range and Multi-phase Signal Generation

Ryoto Fukuda and Mahfuzul Islam
Institute of Science Tokyo, Japan

PS-6 (168)

A Resistor-Based CMOS Temperature Sensor Using a Passive Noise-Shaping SAR ADC

Hohyeop Seo and Jaemyung Lim
Hanyang University, Korea

PS-7 (214)

A 5.8-GHz Class-B LC-VCO Using Inductive Tail Source Degeneration for Phase Noise Reduction

Juchan Lee, Sunyong Choi, Howon Kim, and Kangyoon Lee
Sungkyunkwan University, Korea

PS-8 (221)

A Wide-Input-Range BGR Circuit Using HV-LDO and Hybrid Compensation

Tzung-Je Lee¹, Pin-Chun Li¹, Aleksandr Vasjanov², and Vaidotas Barzdenas²

¹*National Sun Yat-Sen University, Taiwan*

²*Vilnius Gediminas Technical University, Lithuania*

POSTER SESSIONS, Oct. 13

Circuits and Systems for Emerging Technologies

PS-9 (59) Parallelizing Quantum Breadth-First Union-Find Decoder with Processing-in-Memory Architecture

Jeonggeun Seo, Dongmin Kim, and Youngsun Han
Pukyong National University, Korea

PS-10 (68) Representative-Via-Based Thermal Modeling With Layer-Wise Anisotropic Blocks for AI Packages

Seungjin Lee¹, Jaeyoung Choi¹, Sungmo Chae², Jae Yong Song², and Jaemyung Lim¹
¹*Hanyang University, Korea*
²*Pohang University of Science and Technology, Korea*

PS-11 (120) An STDP-Based Learning Circuit for Winner-Take-All in a Neuron-Synapse Array

Haelyn Choi, Joon Young Kwak
Ewha Womans University, Korea

PS-12 (131) CMOS System Design for Memristor-Based Neuromorphic Hardware Verification

Chaei Lee, Ria Choi, and Joon Young Kwak
Ewha Womans University, Korea

PS-13 (141) Design-Parameter Effects on VTF Metrics of RDL Lines in Glass Interposers

Donghyun Uhm, Sumin Lee, Jaemyeong Kang, and Jaemyung Lim
Hanyang University, Korea

PS-14 (142) Accelerating Sequence Alignment with UPMEM PIM Systems

Seongmin Kim, Myeongjin Kwak, and Yongtae Kim
Kyungpook National University, Korea

PS-15 (161) HEAD: A 12-nm Domain-Partitioned Automotive SoC with Silicon-to-Vehicle Demonstration

Moonteol Kee¹, Heesung Shin¹, Gun Woo Lee¹, Kibeen Hong¹, Seungpil Shim¹, Yoomi Park², Jung Hwan Choi³, Youngwoo Kim⁴, Kyungho Kim⁵, and Youngkuk Oh⁶
¹*Supergate Co., Ltd., Korea*
²*Electronics and Telecommunications Research Institute, Korea*
³*Openedges technology, Inc., Korea*
⁴*Btree Co., Ltd., Korea*
⁵*Korea Electronics Technology Institute, Korea*
⁶*DNV Business Assurance Korea, Korea*

POSTER SESSIONS, Oct. 13

PS-16 (171) Cryogenic Miller Op-Amp Utilizing Reconfigurable Field-Effect Transistors

Julian Kulenkampff¹, Andreas Fuchsberger², Paul Krajczek², Lukas Wind²,
Walter M. Weber², Masiar Sistani², and Klaus Hofmann¹

¹Technical University of Darmstadt, Germany

²Technische Universität Wien, Austria

PS-70 (163) A Monolithic GaN 48V-to-1V Buck Converter With an Integrated Feedback Controller

Junho Cho, Donghun Kim, and Jongsun Kim

Hongik University, Korea

Data Converters

PS-17 (9) Design of a High-Speed Time-Domain SAR ADC for High-Speed Receivers

KyungJoon Lee, EuiChan Song, and Jaeduk Han

Hanyang University, Korea

PS-18 (54) Prediction-based timing-calibration technique for time-interleaved ADC

Sang-Won Oh, Hyeon-Gi Hwang, Yoon-Seo Jang, and Dong-Ryeol Oh

Jeju National University, Korea

PS-19 (55) 6-b 10-MS/s V-I SAR ADC

Jimin Kim, Yewon Yoon, Woosuk Shin, and Dongryeol Oh

Jeju National University, Korea

PS-20 (187) A 6-bit 10-GS/s Current-Steering DAC in 28-nm CMOS

Yoon-Seo Jang and Dong-Ryeol Oh

Jeju National University, Korea

PS-21 (191) A Passive Noise-Shaping SAR ADC With Capacitor-Reconfigured Input Summation

Ye-Won Yoon and Dong-Ryeol Oh

Jeju National University, Korea

POSTER SESSIONS, Oct. 13

Digital Circuits, Architecture, and Systems

PS-22 (19)

STAG: Systolic-Array Trajectory Authentication Guard for Secure AI Accelerator Test

Dayoung Kim, Sooryeong Lee, Seungtae Kim, Nuri Son, and Sungho Kang
Yonsei University, Korea

PS-23 (22)

SyncECC: Coordinated ECC Protection Across Storage and Transfer Errors in LPDDR6

Seunghyun Kim, Junhwan Kim, and Jung-rae Kim
Sungkyunkwan University, Korea

PS-24 (32)

A Fully Synthesizable Time-to-Digital Converter for Cost-Efficient Hardware Design

Byeonggeun Kim, Aryeo Roh, Seung Hwa Park, and Jongmin Lee
Ajou University, Korea

PS-25 (34)

Designing FP-INT DRAM Processing-in-Memory Architecture for Edge LLM Inference

Sanghyeok Han and Jae-Joon Kim
Seoul National University, Korea

PS-26 (35)

A High-Speed Reduced-Candidate ACS Look-Ahead Viterbi Decoder Design for 112 Gbps SerDes Systems

Shin-Chi Lai¹, Li-Chuan Hsu¹, Wei-Da Chen², Wei-Zen Chen³, Ming-Hwa Sheu², and Shin-Chang Hsia²

¹National Formosa University, Taiwan

²National Yunlin University of Science and Technology, Taiwan

³National Yang Ming Chiao Tung University, Taiwan

PS-27 (74)

Codec-Inspired Lossless Tensor Compression for Reducing DRAM-SRAM Traffic in Edge NPU Accelerators

Minseo Lee and Munhyeon Kim
Seoul National University, Korea

PS-28 (75)

Characterizing the Impact of Caching Granularity on CXL DRAM Cache Performance

Taeyeon Song, Boyeol Choi, and Jung-rae Kim
Sungkyunkwan University, Korea

POSTER SESSIONS, Oct. 13

PS-29 (82)

Hardwired Spatial Reversal for Stochastic Spiking Neural Network Accelerators

Minkyung Kim and Youngmin Kim
Hongik University, Korea

PS-30 (101)

A Single LFSR XOR-MUX Stochastic Number Generator with SCC Reduction Unit

Kaeun Lim and Youngmin Kim
Hongik University, Korea

PS-31 (126)

Initial-State-Dependent Backup Switching Behavior in Ferroelectric Static Random-Access Memory

Seungmin Jun and Jongwook Jeon
Sungkyunkwan University, Korea

PS-32 (146)

Density-Constrained Offset Selection for INT4 SRAM-CIM Weight Encoding

Minju Kang and Munhyeon Kim
Seoul National University, Korea

PS-33 (166)

Beyond System Compromise: A Methodology for Auditing and Remediating Privilege-Escalation Risk on Edge-AI SoC Platforms

Li-Yu Liu¹, Chin-Fu Nien¹, Yi-Chang Wang², Po-Ling Sun², Wan-Chen Hou², Wen-Kuei Lai², and Kuo-Shu Luo²

¹National Yang Ming Chiao Tung University, Taiwan

²Industrial Technology Research Institute, Taiwan

PS-34 (172)

Metric 3D Height Reconstruction from 2D SEM Images via Confidence-Weighted Fusion of Stereo and Four-Channel Photometric Cues

Junseo Bang¹, Jason Park¹, Yoontaek Han², Seulki Roh², Yujin Cho², Mingi Kang², and Se Young Chun¹

¹Seoul National University, Korea

²Samsung Electronics Co., Ltd., Korea

PS-35 (193)

RA-PRAC: Restore-Aware Proactive Mitigation Target Selection for PRAC

Younghun Kang and Hayoung Lee
Ajou University, Korea

POSTER SESSIONS, Oct. 13

Machine Learning and AI

PS-36 (23)

Low-Resolution Two-Frame Depth Prediction for Distance-Aware Vision

Jiyeon Hong and Jinwook Burm
Sogang University, Korea

PS-37 (45)

A High-Accuracy, Hardware-Efficient RoPE Accelerator for Long-Context Edge LLMs

Ting-Yu Chuang, Yao-Chen Kuo, Kai-Yi Hu, and Jinn-Shyan Wang
National Chung Cheng University, Taiwan

PS-38 (46)

Toward Hardware-Intrinsic Individuality Using Reservoir for Edge AI Computing

Masahiro Ogawa, Shintaro Takenaka, and Takeshi Kumaki
Ritsumeikan University, Japan

PS-39 (58)

Development of an AI-Based Autonomous Feeding System for Land-Based Aquaculture

Tsubasa Hibino and Takeshi Kumaki
Ritsumeikan University, Japan

PS-40 (113)

FlexRot: A Flexible Hadamard Rotation Module for Non-PoT Dimensions in Low-Bit LLM Inference

Junha Ko, Inseong Hwang, and Hyun Kim
Seoul National University of Science and Technology, Korea

PS-41 (115)

Lane-Aware Self-Recovery Architecture for Column-Based Digital PIM

Yunje Hwang and Hayoung Lee
Ajou University, Korea

PS-42 (134)

Design-Space Exploration of EMA-Based Gradient-Free SNN Training on MNIST

Seoyoon Park and Youngmin Kim
Hongik University, Korea

PS-43 (195)

StatNet: Physics-in-the-Loop Learning of Observation Statistics for RSS-Only mmWave Array Calibration

Jeeshoo Kim, Donggyun Kim, Seunga Hong, and Kangyoon Lee
Sungkyunkwan University, Korea

POSTER SESSIONS, Oct. 13

PS-44 (212)

Trading Bit Errors for Link Power in LLM Memory Interfaces

Yunhoe Koo and SeongHwan Cho

Korea Advanced Institute of Science and Technology, Korea

PS-45 (254)

A Novel Low-Power Time-Domain Computing-In-Memory Microarchitecture for Edge-AI

Yixuan He¹, Minsu Choi², Kyung Ki Kim³, and Yong-Bin Kim¹

¹*Northeastern University, USA*

²*Missouri University of Science & Technology, USA*

³*Daegu University, Korea*

PS-46 (258)

Adaptive Approximate Stochastic Computing for Low-Power AI Inference on Edge Devices

Keerthana Pamidimukkala¹, Kyung Ki Kim², Yong-Bin Kim³, and Minsu Choi²

¹*Missouri University of Science & Technology, USA*

²*Daegu University, Korea*

³*Northeastern University, USA*

PS-47 (295)

Corner-Aware Surrogate Modeling of a Subthreshold PTAT/CTAT CMOS Voltage Reference Circuit

Ashutosh Singh, Shivani, Anuj Grover, and Sonia Bondwal

Indraprastha Institute of Information Technology Delhi, India

POSTER SESSIONS, Oct. 13

RF/Wireless

PS-48 (53)

Graph Attention Network-Based Surrogate Modeling of PA Output Matching Networks

Won-Hyung Park, Ji-Sung Jang, and Kang-Yoon Lee
Sungkyunkwan University, Korea

PS-49 (76)

A 28-GHz CMOS Down-Conversion Mixer with Magnetically Coupled Source Degeneration Inductors

Yo Sceph Kim, Jin Man Myung, Geonwoo Park, Ho Kim, Suyeon Lee, and Ilku Nam
Pusan National University, Korea

PS-50 (167)

Injection-locked Frequency Doubler in GaN HEMT Process

Mao-Hsiu Hsu¹, Sheng-Lyang Jang², Yong-Jun Chang³, and Wen-Cheng Lai²
¹*National Formosa University, Taiwan*
²*Ming Chi University of Technology, Taiwan*
³*National Taiwan University of Science and Technology, Taiwan*

PS-51 (183)

An RF-Filtering CG–CS Noise-Cancelling LNA with Current-Reuse Q-Boosted LC Notch Filter for 5G New Radio Cellular Applications

Jeongmin An, Donggu Lee, Heesu Lee, and Kuduck Kwon
Kangwon National University, Korea

PS-52 (184)

A 5–9 GHz Low-Power Receiver Front-End Using Current-Reuse gm-boosting and Current-Bleeding Techniques for 6G FR3 Cellular Applications

Byounghyun You, Sejin Lee, Sukju Yun, and Kuduck Kwon
Kangwon National University, Korea

PS-53 (203)

A Blocker-Tolerant N-Path Balun-LNA Adopting a Frequency-Selective Regulated Common-Gate Stage for Reliable Drone Communication

Jungseob Lim, Back Lee, Siwoong Park, and Donggu Im
Jeonbuk National University, Korea

PS-54 (242)

A High-Isolation 140-GHz Silicon-Lens-Integrated Differentially Fed On-Chip Slot Antenna for In-Band Full-Duplex Applications

Atiq Ben Ahmed and Munkyo Seo
Sungkyunkwan University, Korea

POSTER SESSIONS, Oct. 13

SoC Design Methodology and CAD

PS-55 (27) Low-Overhead Partial Enhanced Scan for Transition Delay Fault Testing

Jaehyun Kim, Dahoon Kim, Hoyeon We, and Sungho Kang
Yonsei University, Korea

PS-56 (64) Exploring LLM-Generated Initial Solutions for Simulated Annealing-Based MPW Reticle Floorplanning

Ching-Yuan Chang, Hui-Lin Cho, Ciao-Ying Su, Yu-Feng Huang, and Yu-Cheng Lin
Yuan Ze University, Taiwan

PS-57 (71) Automated Design Framework for Capacitive Receiver Transimpedance Amplifiers via TuRBO

Sanghoon Lee¹, Youngchan Jo¹, F. Levent Degertekin², and Jaemyung Lim¹
¹*Hanyang University, Korea*
²*Georgia Institute of Technology, USA*

PS-58 (105) GraphSAGE-Based Partial Scan Flip-Flop Selection for High Test Coverage

Taehyun Kwak¹, Jin Hwan Park², Minsuk Sung³, and Young-woo Lee²
¹*Inha University, Korea*
²*Teradyne Inc., USA*
³*Tanhay Inc., Korea*

PS-59 (114) Lane-Aware Self-Test Architecture for Column-Based Digital PIM

Yunje Hwang and Hayoung Lee
Ajou University, Korea

PS-60 (118) Exploiting Additive Delay Structure for Seven-Point SRAM NLDM Reconstruction

Aiganyam Zhalinova and Hanwool Jeong
Yonsei University, Korea

PS-61 (125) Hardware-Software Co-Optimization Techniques for Compute-in-Memory CNN Inference

Joonhyeok Yeom and Eui-Young Chung
Yonsei University, Korea

PS-62 (143) Detecting Stale-Data Write Suppression in an SRAM Using ML on Simulation Collaterals

Surajit Bhattacharjee and Dipankar Pal
Birla Institute of Technology & Science Pilani, India

POSTER SESSIONS, Oct. 13

PS-63 (181)

Pareto-Guided Model Selection for SAT Runtime Prediction: Balancing RMSE and Macro-F1Rui Ma¹, Haimin Yan¹, Tomohisa Kawakami², Tomoyasu Shimada¹, Xiangbo Kong³, Hiroyuki Tomiyama¹, and Shigeru Yamashita¹¹*Ritsumeikan University, Japan*²*Duke University, USA*³*Toyama Prefectural University, Japan*

PS-64 (218)

ChipNexus: Closed-Loop LLM-Orchestrated EDA for MEMS-ASIC Multi-Chip AssemblyYuchi Zou¹, Jing Zhang², Longyang Lin³, Yan Su², Yongfu Li¹, and Jian Zhao²¹*Shanghai Jiao Tong University, China*²*Nanjing University of Science and Technology, China*³*Southern University of Science and Technology, China*

Wireline

PS-65 (130)

A 5-Gb/s/TSV Feedback N-N Driver with Effective VOH Drift Suppression for HBM I/O Interfaces

Hyeun Cho and Won-Young Lee

Seoul National University of Science and Technology, Korea

PS-66 (132)

A 30-Gb/s PAM-3 Receiver with Single-Sample ZUI Decoder for High-Speed Memory Interfaces

Haesu Shin and Won-Young Lee

Seoul National University of Science and Technology, Korea

PS-67 (162)

A Wide-Range All-Digital PLL Employing a Triple Phase Detection Scheme for Dynamic Frequency Scaling

Taeil Song and Jongsun Kim

Hongik University, Korea

PS-68 (199)

A 24 Gb/s 0.55 pJ/bit PAM-3 Transmitter for Static Current Elimination

Mingyun Kim, Myeongju Park, Jongchan An, Seung-Myeong Yu, Gyuwon Jeon, Yoonsang Lee, Gwangmyeong An, Songi Cheon, and Junyoung Song

Incheon National University, Korea

Undergraduate Research Exhibition Fair

PS-69 (185)

An Event-Driven 10T SRAM CIM Circuit for Low-Power Wearable Pediatric Wheeze Detection

Taerin Lee, Jiwoo Song, Yejin Lee, Yubin Lee, Subin Hwang, and Jongyoon Choi

Ewha Womans University, Korea

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CHIP DESIGN CONTEST

MONDAY, OCTOBER 12

CDC Oral Session

Chair: Seonghwan Cho (KAIST, Korea)

08:40~10:10, MONDAY_OCTOBER 12, 2026
201+202 (2F)

CDC-O001

08:40-08:55

A Low-Jitter Fractional-N Digital PLL Using a Quantization-Error-Compensating BBPD and an Orthogonal-Polynomial-Based LMS Calibration

Munjae Chae, Seheon Jang, Seungjae Lee, and Jaehyouk Choi
Seoul National University, Korea

CDC-O002

08:55-09:10

A Low-Power and Compact IEEE 802.15.4a/z/ab-Compliant IR-UWB Transmitter with Enhanced Spectrum Utilization and Sidelobe Suppression

Jihun Son, Chansoo Park, and Minyoung Song
Daegu Gyeongbuk Institute of Science and Technology, Korea

CDC-O003

09:10-09:25

A Hybrid Bidirectional Converter with Normalized-Inductor-Current Based Adaptive Target Current Tracking Achieving 97.4%-Peak-Efficiency

Yunho Lee, Changwook Ahn, and Hyung-Min Lee
Korea University, Korea

CHIP DESIGN CONTEST

CDC-O004 A 88-Gb/s PAM-4 DSP-DAC Transmitter with LUT-Based Equalization

09:25-09:40 Dongho Kim, Seung-Mo Jin and Min-Seong Choo
Hanyang University, Korea

CDC-O005 A Fully Integrated Electromagnetically Coupled Recursive Resonant Switched-Capacitor Converter with Tri-coupled Inductor

09:40-09:55 Taehyeong Park, Jibeom Lee, and Chulwoo Kim
Korea University, Korea

CDC-O006 A 12-Gb/s PAM-3 Receiver with Area-and Energy-Efficient Sub-Baud-Rate CDR Employing a VREF-Modulated Comparator and Achieving 0.67 Pattern Utilization

09:55-10:10 Chaehyeon Lim and Joo-Hyung Chae
Kwangwoon University, Korea

CDC Live Demo

08:40~17:40, MONDAY_OCTOBER 12, 2026
LOBBY (2F)

CDC-D001 A Low-Jitter Fractional-N Digital PLL Using a Quantization-Error-Compensating BBPD and an Orthogonal-Polynomial-Based LMS Calibration

Munjae Chae, Seheon Jang, Seungjae Lee, and Jaehyoun Choi
Seoul National University, Korea

CDC-D002 A Low-Power and Compact IEEE 802.15.4a/z/ab-Compliant IR-UWB Transmitter with Enhanced Spectrum Utilization and Sidelobe Suppression

Jihun Son, Chansoo Park, and Minyoung Song
Daegu Gyeongbuk Institute of Science and Technology, Korea

CDC-D003 A Hybrid Bidirectional Converter with Normalized-Inductor-Current Based Adaptive Target Current Tracking Achieving 97.4%-Peak-Efficiency

Yunho Lee, Changwook Ahn, and Hyung-Min Lee
Korea University, Korea

CHIP DESIGN CONTEST

CDC-D004

A 88-Gb/s PAM-4 DSP-DAC Transmitter with LUT-Based Equalization

Dongho Kim, Seung-Mo Jin and Min-Seong Choo
Hanyang University, Korea

CDC-D005

A Fully Integrated Electromagnetically Coupled Recursive Resonant Switched-Capacitor Converter with Tri-coupled Inductor

Taehyeong Park, Jibeom Lee, and Chulwoo Kim
Korea University, Korea

CDC-D006

A 12-Gb/s PAM-3 Receiver with Area-and Energy-Efficient Sub-Baud-Rate CDR Employing a VREF-Modulated Comparator and Achieving 0.67 Pattern Utilization

Chaehyeon Lim and Joo-Hyung Chae
Kwangwoon University, Korea

CDC Poster Session

Chair: Seonghwan Cho (KAIST, Korea)

08:40~17:40, MONDAY_ OCTOBER 12, 2026
LOBBY (2F)

CDC-P001

SPAD Array Design for iToF LiDAR System

Jonghyuk Chae, Jiyeon Hong, and Jinwook Burm
Sogang University, Korea

CDC-P002

Yield-Aware System-Level Design and Optimization of a 12.5-bit-ENOB Second-Order Noise-Shaping SAR ADC for Battery Management Systems

Dongwoo Seo, SangHyun Kwak, and Cheonhoo Jeon
Dankook University, Korea

CDC-P003

An 85.5-to-94.5-GHz W-Band Fully-Symmetric Quadrature LO Generator with a Fast Quadrature Calibration Technique, Achieving Closely Matched 61-fs RMS Jitter and 41-dB IRR

Sarang Lee, Seohee Jung, Seohyeon Kwak, Seungjae Lee, Hoojung Lee, and Jaehyouk choi
Seoul National University, Korea

CDC-P004

An 11-ns-Locking 4–8-GHz Closed-Loop Analog Duty-Cycle Corrector With an Embedded Set Generator

Songl Cheon and Junyoung Song
Incheon National University, Korea

CHIP DESIGN CONTEST

CDC-P005**10-40 GHz 28nm SOI CMOS Wideband LNA**

Hosung Kang, Bonhyeok Gu, Juyoung Kim, Yuseok Ban, and Jihoon Kim
Kyonggi University, Korea

CDC-P006**High performance SOI CMOS Broadband Cascode Frequency Downconverter**

Hosung Kang, Um Yoojung, Lee Yeonwoo, and Jihoon Kim
Kyonggi University, Korea

CDC-P007**A 16 Gb/s Single-ended PAM-4 Transmitter with Charge-Steering Equalizer**

Mingyun Kim, Myeongju Park, Gyuwon Jeon, Hyanghee Park, and Junyoung Song
Incheon National University, Korea

CDC-P008**A 0.044-mm² 15–19-GHz Type-I Sampling PLL Achieving 42.4-fs Jitter and –257.9-dB FoM With Fast Coarse Locking Loop**

Seunghoon Yi, Yoochang Kim, and Young-Ha Hwang
Soongsil University, Korea

CDC-P009**Discrepancy Between Simulated and Measured Performance in a D-Band CMOS LNA: Layout-Induced Parasitic Analysis**

Jae-Hyeon Lee, Ga-Eun Lee, Tae-Hyung Lee, Hyeon-Woong Shin, and Jong-Ryul Yang
Konkuk University, Korea

CDC-P010**Sub-6 GHz Driverless Direct-Conversion Transmitter in 65nm CMOS Technology**

Jeheon Lee, Donghwi kang, Soo-jin Park, Sung-uk We, and Ji-seon Paek
Pusan National University, Korea

CDC-P011**Small-Area, High-Speed, and High-Uniformity Column Driver IC for OLED-on Silicon (OLEDoS) Displays**

Chong-Hwa Bae, Hyeon-Ho Park, Dong-Kun Lee, and Jong-Seok Kim
Hanyang University ERICA, Korea

CDC-P012**Smart Meter SoC with Adaptive Calibration for Smart Cities**

Ji-Soo Seo, Jae-Lim Lee, and Dong-Sun Kim
Sejong University, Korea

CHIP DESIGN CONTEST

CDC-P013

A 48-Channel Time-Interleaved SAR ADC with Hierarchical Rank1/2 Sampling for Wireline Receivers

Hyeon-woo Kim, Hyung-jun Kim, Jae-yoon Lee, and Min-jae Seo
University of Seoul, Korea

CDC-P014

48-way PAM-4/8 Reconfigurable DSP-based receiver in 28nm CMOS Technology

Jae-Geon Lee¹, Seung-Mo Jin¹, Joon-Seok Kwon¹, and Min-Seong Choo²
¹*Hanyang University, Korea*
²*Yonsei University, Korea*

CDC-P015

A Capacitive-Latch TRNG Featuring Both Autozeroed Inverter Mismatch and Accelerated Evaluation

Woojin Lee and Chulwoo Kim
Korea University, Korea

CDC-P016

An End-to-End Simultaneous Speech Translation Processor on Edge Devices

Bokyoung Seo¹, Ghangmin Yun², Chaeyoon Kim², Junghyun Yoo², and Kyuho Lee²
¹*Ulsan National Institute of Science and Technology, Korea*
²*Yonsei University, Korea*

CDC-P017

A Fully Integrated Domino-Like Buffer FVF LDO with fast transient response

Taehyun Kim, Chanbin Hwang, and Junyoung Song
Incheon National University, Korea

CDC-P018

A 10 GHz Digital PLL Employing Pseudo-Differential DTC for DTC Cover Range Reduction

Changmin An and Heein Yoon
Ulsan National Institute of Science and Technology, Korea

CDC-P019

Design of a 1.5-GS/s 6-bit Loop-Unrolled SAR ADC Utilizing Speculative CDAC Switching in 28-nm CMOS

Hyeon-Seo Kim¹ and Min-Seong Choo²
¹*Hanyang University, Korea*
²*Yonsei University, Korea*

CDC-P020

A CMOS Image Sensor ROIC with 1550-nm Infrared Quantum-Dot Photodiodes

Hongju Lee, Hyo Cheol Ahn, Sehyeon Kim, and Yong Sin Kim
Korea University, Korea

CHIP DESIGN CONTEST

CDC-P021

A High-Density 4T-3C eDRAM based Processing-In-Memory for Energy-Efficient Ternary Neural Network Acceleration

Juheon Lee, Gyumin Noh, Jungu Kang, Hyerim Kim, and Yeongkyo Seo
Inha University, Korea

CDC-P022

Design of a 15–23-GHz 5-Bit Switched-Type Phase Shifter in 28-nm SOI CMOS

Seong-Uk Kang, Min-Seok Baek, Byung-Chan Lee, and Choul-Young Kim
Chungnam National University, Korea

CDC-P023

A Wideband Current-Reuse LNA With Transformer-Based Matching in 28-nm CMOS SOI for Millimeter-Wave Receivers

Jong-Seong Park, Min-Seok Baek, Ilhun Kim, Seong-Uk Kang, and Choul-Young Kim
Chungnam National University, Korea

CDC-P024

A Compact 17–22 GHz 5-Bit Switched-Type Phase Shifter in 28-nm CMOS

Jong-Seong Park, Joon-Hyung Kim, Byeong-chan Lee, Ilhun Kim, and Choul-Young Kim
Chungnam National University, Korea

CDC-P025

Quantum-Inspired Hybrid Adiabatic Annealing Processor for Solving Combinatorial Optimization Problems

Taihyun Kim, Hyunjin Kim, Hyundo Jung, Woojin Lee, Jinwoo Jeon, and Chulwoo Kim
Korea University, Korea

CDC-P026

A 24Gb/s Switched-Capacitor Pre-Emphasis for PAM-3 Transmitter with Transition-Level Adaptation

Gwangmyeong An, Gyuwon Jeon, and Junyoung Song
Incheon National University, Korea

CDC-P027

An Always Multi-Path Hybrid DC-DC Converter for IoT Application

Mingi Jeong, Taehyeong Park, and Chulwoo Kim
Korea University, Korea

CDC-P028

Time-based ADC with gated ring oscillator TDC

Jaemin Lee and Gain Kim
Daegu Gyeongbuk Institute of Science and Technology

CHIP DESIGN CONTEST

CDC-P029

Design of 32-Way Signal Distribution Network for High-Speed ADC-DSP Based SerDes

Woojung Park and Gain Kim

Daegu Gyeongbuk Institute of Science and Technology

CDC-P030

A design of Compact Single-Ended Receiver With Graphical User Interface based Analog Layout Generators

Minseo Kim, Chanhyong Lee, Jiyun Lee, and Byungsub Kim

Pohang University of Science and Technology, Korea

CDC-P031

A 1.5 GHz Fully Integrated 4:1 Fully Soft-Charging DC-DC Converter Based on Complementary Electromagnetically Coupled Class-D LC Oscillators with Multi-Coupled XFMRs

Taehyeong Park and Chulwoo Kim

Korea University, Korea

CDC-P032

A Charge-Domain 4T2C eDRAM Compute-In Memory Macro with Enhanced Variation Tolerance and Low-Overhead Data Conversion Schemes

In-Jun Jung¹, Do Han Kim¹, Minyoung Jo¹, Dong Han Ko¹, Youngkyu Lee¹, and Seong-Ook Jung^{1,2}

¹*Yonsei University, Korea*

²*Articron Inc., Korea*

CDC-P033

Area-Efficient FP16 PIM Accelerator with 1T-1C eDRAM in 28nm CMOS

Akshay Kumar Sharma, Byeong-Ho Kang, and Kyung Ki Kim

Daegu University, Korea

CDC-P034

Biphasic Deep Brain Stimulation System Using Adaptive Supply Control

Hojae Chon, Joonghoon Kang, and Hyung-Min Lee

Korea University, Korea

CDC-P035

Inverter-Based CTLE for High-Speed Wireline Receiver Datapath

Dongryul Heo, Hawon Yun, and Gain Kim

Daegu Gyeongbuk Institute of Science and Technology, Korea

CDC-P036

An ECRAM-Based Analog Neuromorphic System with High-Precision Current Readout

Minil Kang¹, Minseong Um¹, Hyunjeong Kwak², Kyungmi Noh², Seyoung Kim², and Hyung-Min Lee¹

¹*Korea University, Korea*

²*Pohang University of Science and Technology, Korea*

CHIP DESIGN CONTEST

CDC-P037

Reliability assessment of 28nm bulk CMOS technology under TID effects

Younghoon Han, Taeyong park, Youngil Kwon, and Gunhee Hong
Yonsei University, Korea

CDC-P038

A Low-Noise Current Reuse OTA and Reference Buffer for Biomedical Signal Acquisition in 28nm FD-SOI CMOS

Md Mossaraf Hossan, Md Turiqul Islam, Gaurav Mehra, Abdey Munaf, Reyad Hossain, Hyunwoo Jin, and Hanjung Song
Inje University, Korea

CDC-P039

A Unified Look-Up-Table Accelerator for the Element-Wise State-Update Loop of State-Space Models

Sunwoo Yoo^{1,2}, Dongyun Kam³, Soonhyun Kwon¹, and Youngjoo Lee¹
¹Korea Advanced Institute of Science and Technology, Korea
²Pohang University of Science and Technology, Korea
³Ulsan National Institute of Science and Technology, Korea

CDC-P040

Design and Implementation of a Spiking Neural Retina Chip for Pattern Recognition Using DB HiTek 180nm BCDMOS Technology

Reyad Hossain, Md Turiqul Islam, Gaurav Mehra, Md Mossaraf Hossan, Tayyab Hasan, Seungwon Kim, and Hanjung Song
Inje University, Korea

CDC-P041

A Capacitor-Less Digital Low Drop-Out Regulator with CNN Inference-based Predictive Controller

Jongwoon Lee, SeungHyun Kang, and In-Chul Hwang
Kangwon National University, Korea

CDC-P042

50MS/s 13-bit Pipelined SAR ADC with 6-Transistor High-Gain Inverter-Based Ring Amplifier in 28nm FDSOI

Hyoseong Kim¹, Yeonghui Kim¹, and Jaehoon Shim²
¹DB GlobalChip Co., Ltd., Korea
²Kyungpook National University, Korea

CDC-P043

An IC-Integrated EIS Measurement System for Online Battery Diagnosis

Sihyun Jung, Ayeon Gwon, and Junwon Jeong
Sookmyung Women's University, Korea

CHIP DESIGN CONTEST

CDC-P044

A Low-Overhead Side-Channel Attack-Resilient LDO for Secure SoCs

Sihyun Jung, Yeseul Song, and Junwon Jeong
Sookmyung Women's University, Korea

CDC-P045

A Dual-Mode 1.2V to 6.0V DC/DC Boost Converter for LCoS Microdisplay Back-plane of XR Glasses

Yeo-jin Lee, Jung-Gi Lee, Sun-Ju Kwon, and In-Chul Hwang
Kangwon National University, Korea

CDC-P046

Multi-Step Pulse – Width Modulator for Low – Power Signal Isolation in Wide Bandgap (WBG) Gate drivers

Donghyun Kim and Minseob Shim
Gyeongsang National University, Korea

CDC-P047

A Low-Power and Low-Area Ultrasound Transceiver SoC for BBB Opening with Adiabatic Charge TX and Envelope Detection RX

Ho Jun Kim, Yu Been Oh, and Jae Myung Lim
Hanyang University, Korea

CDC-P048

Machine Learning Model-Based On-Chip Inductor Inverse Design

Naeun Kim, Uichan Park, Sangjoon Oh, and Seongwoog Oh
Seoul National University, Korea

CDC-P049

Design of an 80-Gb/s PAM4 Receiver Analog Front-End for High-Speed SerDes in 28-nm CMOS

Hojun Chung¹, Changjae Moon², Jiyun Lee¹, Seokhoon Kim¹, and Byungsub Kim¹
¹Pohang University of Science and Technology, Korea
²University of California, Berkeley, USA

CDC-P050

Radiation-Tolerant Continuous-Time Pipeline ADC with Delay Matching via DAC Injection Point and SEE-Tolerant Pseudo-Differential Comparator

Charlie Tahar and Seung-Tak Ryu
Korea Advanced Institute of Science and Technology, Korea

CDC-P051

A K-Band Linear Power Amplifier Using pMOS Varactor and Harmonic Trap in 28-nm SOI

Ilhun Kim¹, Joon-Hyung Kim¹, Jong-Seong Park¹, Seong-Uk Kang¹, Gwang-Hyeon Jeong², and Choul-Young Kim¹
¹Chungnam National University, Korea
²Hanbat National University, Korea

CHIP DESIGN CONTEST

CDC-P052

Design of a 17.7–21.2 GHz Low-Noise Amplifier for Satellite Communications

Byeong-Chan Lee¹, Jeong-Taek Son¹, Jong-Seong Park¹, Gwang-Hyeon Jeong², and Choul-Young Kim¹

¹*Chungnam National University, Korea*

²*Hanbat National University, Korea*

CDC-P053

An Efficient Negative Voltage Generator for Compact and High-Temperature Operation

Taegun Yim, Choongkeun Lee, Suna Lee, and Hongil Yoon

Yonsei University, Korea

CDC-P054

A Low Power Sense-Amplifier-Based Flip-Flop using Floating Node Elimination Technique

Taegun Yim, Choongkeun Lee, Suna Lee, and Hongil Yoon

Yonsei University, Korea

CDC-P055

A 6GHz Cascode Class-J Power Amplifier with Second-Harmonic Control in 180nm CMOS

Woo-Hyun Go and Jung-Dong Park

Dongguk University, Korea

CDC-P056

A 6.78-MHz Wireless Power Receiver with Single-Stage 3-Mode Active Rectifier and Precision Ramp Control

Junyoung Heo, Dohyun Shin, and Jinwook Burm

Sogang University, Korea

CDC-P057

Efficient Digital Computing-In-Memory Macro with No-Accuracy Loss

Wonkyung Han, Jaeyong Jang, Jihoon Park, Sooah Choi, Dohyun Kim, Juheun Lee, and Jae-Joon Kim

Seoul National University, Korea

CDC-P058

PWM-ASK Receiver Supporting High Supply Variation Tolerance and High Order Modulation

Jungwon Kwun and Jaeeun Jang

Kwangwoon University, Korea

CHIP DESIGN CONTEST

CDC-P059

High-Speed Synthesizable Multi-Point Temperature Sensor

Seokhyun Jung and Wanyeong Jung
Korea Advanced Institute of Science and Technology, Korea

CDC-P060

A 77–81 GHz W-Band CMOS Receiver with Bypass-Enabled Block-Level Verification for Short-Range Radar

Ilhun Kim, Jae-Hyeok Song, Jong-Seong Park, Seong-Uk Kang, and Choul-Young Kim
Chungnam National University, Korea

CDC-P061

A CMOS Bidirectional Active Mixer for 5G FR2 Applications

Juhui Jeong and Junghwan Han
Chungnam National University, Korea

CDC-P062

A 0.00287 mm² 4 GS/s 8-bit Time-Interleaved SAR ADC With Information-Rate-Density Analysis

Woo-Jin Jeon, Beom-Yeon Cho, and Chan-Ho Kye
Gachon University, Korea

CDC-P063

A 180-nm Analog Leaky-Integrate-and-Fire Neuron for Battery-Free Always-On Neuromorphic Tags

Heonho Shin and Song Min Kim
Korea Advanced Institute of Science and Technology, Korea

CDC-P064

Phase Noise Reduction in Ring VCOs Using Adaptive AC-Coupled Delay Cells

Geonwoo Park¹, Donggu Im², and Ilku Nam¹
¹*Pusan National University, Korea*
²*Jeonbuk National University, Korea*

CDC-P065

A 24/48V-to-PoL Interposed-Stacking Multi-Phase Hybrid Buck Converter with Auto VCF and IL Balancing

Ji-Hoon Bang¹, Sang-Gug Lee¹, and Kyung-Sik Choi²
¹*Korea Advanced Institute of Science and Technology, Korea*
²*Yonsei University, Korea*

CDC-P066

A 110-160 GHz Wideband Two-stage Cascode Power Amplifier in 250-nm InP HBT Technology

Jeongho Baek and Jinho Jeong
Sogang University, Korea



CLOSING CEREMONY

CLOSING CEREMONY

TUESDAY, OCTOBER 13



17:00~17:30 TUESDAY, OCTOBER 13, 2026
Premier Ballroom (2F)

Best Paper Awards

Best Poster Awards

Gift Drawing

DISCUSSION

DISCUSSION

WEDNESDAY, OCTOBER 14

10:00~11:00 WEDNESDAY, OCTOBER 14, 2026

SPECIAL PROGRAMS

Banquet

- **Banquet** at Songdo ConvensiA will be provided to **all the on-site registrants** after the afternoon sessions **on Oct. 12**, respectively.

Date	Monday, Oct. 12, 2026
Time	18:00-20:00
Venue	Premier Ballroom A+B (2F)

The venue for the banquet is “**Premier Ballroom**”, main conference venue.

- Please make sure that you have to show the **Banquet coupon in your name badge**. Conference attendee will get a banquet coupon together with the conference admission badge. Please be noted that you have to keep the coupon well and show it to the staff when having Banquet.
- All the conference registration includes an admission ticket for banquet.
- This year, Additional Banquet tickets are not available on site.

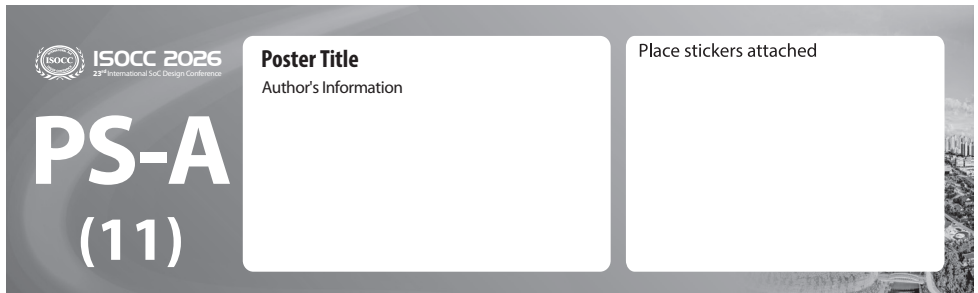
SPECIAL PROGRAMS

Most Popular Poster Voting

- **All on-site registrants** can vote by putting a small sticker on the **“Place stickers here”** above each ISOCC Poster. More than one sticker can be added to any posters.
- Inside your name tag, you will find **two stickers** that can be used for this voting.
- Valuable gifts will be awarded at **the Closing Ceremony to the top-5 popular ISOCC Posters.**

Date	Tuesday, Oct. 13, 2026
Time	17:00-17:30
Venue	Premier Ballroom (2F)

(Sample Image)



SPECIAL PROGRAMS

Gift Drawing

- **Gift Drawing** for conference attendees will be held during the **Closing Ceremony**.

Date	Tuesday, Oct. 13, 2026
Time	17:00-17:30
Venue	Premier Ballroom (2F)

(Sample Image)



Nintendo Switch2



Samsung Galaxy Watch 9



Samsung Galaxy Bud4 Pro

SPECIAL PROGRAMS

Gift for Session Participants

- A sticker for each attendee will be provided by our session staff at the end of each session including Tutorials, Short Tutorials, and Company Exhibition.
- We present **Special gift** based on the number of stickers. Please do not miss this chance.
- You can receive the **gift at the registration desk**.

Date	Programs	Slot Completion Condition	Gift Claim Condition
Oct. 11 (Sun.)	- Main Tutorials - Short Tutorials	More than 2 Stickers for each slot	Complete more than 3 slots.
Oct. 12 (Mon.)	- CDC Oral Session - Keynotes Speeches		
	- Afternoon Session-1 - Afternoon Session-2 - Company Exhibition/Demo		
	- Morning Session - Keynotes Speeches		
Oct. 13 (Tue.)	- Afternoon Session-1 - Afternoon Session-2		

- * All stickers must have different colors/shapes.
- * Gifts are offered on a first-come, first-served basis, so it can be sold out early.



CONFERENCE INFORMATION

Lunch

- **Lunch** at Songdo ConvensiA will be provided to **on-site registrants** after the morning sessions on **Oct. 12 and Oct. 13**, respectively.

Date	Monday, Oct. 12, 2026	Tuesday, Oct. 13, 2026
Time	12:20 - 13:40	12:00 - 13:20
Venue	Restaurant in Songdo ConvensiA (1F)	

- Please make sure that you have to show the **lunch coupon in your name badge**. The coupon can be used at designated restaurants on the 1st floor of Songdo ConvensiA for meals up to KRW 15,000.
- Any amount exceeding KRW 15,000 must be paid individually.

Coffee Break

Coffee and Cookies will be served at the following hours.

Date	Monday, Oct. 12, 2026	Tuesday, Oct. 13, 2026
Time	10:10-10:15 14:55-15:10	10:00-10:10 14:35-14:50
Venue	Premier Ballroom (2F) Lobby	

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- If you want to download the file to your USB or external drive, please ask our staffs at the registration desk.
- Please use your PC/MAC/Laptops for full access. (Not Accessible through smartphones)

CONFERENCE INFORMATION

Emergency Calls

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Fire, Rescue & Hospital Services	119
Non-urgent Medical	129
Korea Travel Helpline	1330
Report Child Abuse	112

- Our Staff will be wearing the uniform(Yellow Vest) shown as below.



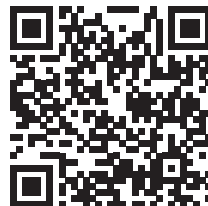


CONFERENCE INFORMATION

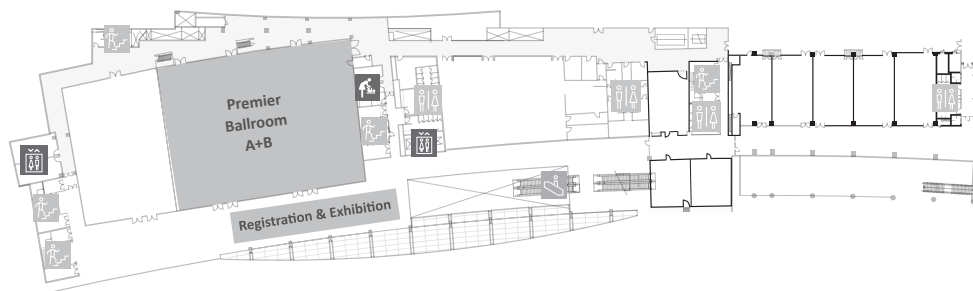
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회사소개

테크위드유 주식회사는 2016년 12월 반도체 개발업, 제조 판매업을 목적으로 설립하여 기술집약적이며, 고품질의 Analog IP 및 제품을 공급하는 국내 Fabless 반도체 설계 회사입니다.

산업용 시스템에서 필요로 하는 고수익 디폴트 아날로그 제품 위주로 개발하고 있으며, 부가적으로 초미세 공정항 아날로그 기반 설계기술의 확보를 통해 Analog IP 들을 국내외 고객에게 제공하고 있습니다.

서비스 및 아이텔 소개

- 1) Mixed-signal IP & Platform
Generic Analog IP (LDO/POR/MLD/ADC 등)
Power management IP (DC-DC Converter 등)
- 2) Industrial Soc
DC Motor Driver IC
Multi-channel PMIC
- 3) Automotive Soc
USB Type-C PD Charger IC
Head Lamp LED Driver IC

복리후생제도

 건강검진 비용 지원 (2인)	 선택적 복리후생 (제약면련, 자기개발 등)
 식사 및 스낵바 제공	 경조사 지원
 장기근속 포상 및 휴가 (만 5년 ↑ 300만원)	 콘도 회원권 운영
 특허 보상금 (출원 50만원 / 등록 100만원, 200만원)	 사내 대출 제도

인공지능 반도체 IP 플랫폼 전문기업

오픈엣지테크놀로지

세계 유일 AI 반도체의 구동 기반이 되는 통합 IP 솔루션 제공:

- NPU IP - 인공지능 학습과 실행에 최적화된 신경망 처리장치
- On-chip Interconnect IP - SoC 내 데이터 이동 통로
- Memory Controller IP - 스케줄링 알고리즘에 따라 SoC와 DRAM 간 고속 데이터 통신을 제어
- DDR PHY IP - SoC와 DRAM 간 고속 데이터 전송

반도체 분야 최초
기술평가 AA등급 취득

세계 유일 AI 반도체
통합 IP 솔루션 제공

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Track Record

글로벌 기업과의
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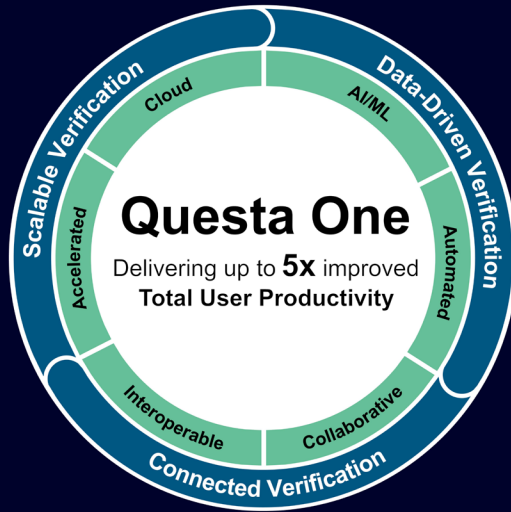
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Heejin.yoon@asicland.com





DIGITAL INDUSTRIES SOFTWARE

Faster engines.
Faster engineers.
Fewer workloads.

Questa One Sim

One engine with breakthrough performance for functional and fault simulation for RTL, GLS and DFT applications with parallel processing and profiling.

Questa One Verification IQ

One smart common coverage solution that utilizes generative, analytic and predictive AI to drive to verification closure faster, with fewer workloads.

Questa One SFV

One stimulus-free verification solution delivers total user productivity through synergistic combinations of static and formal analyses, AI, automation and parallelization.

Questa One Avery Verification IP

One industry-leading VIP solution that supports 3DIC and chiplet verification from IP to SoC, seamlessly integrating simulation and emulation.

siemens.com/questa



SIMetrix / SIMPLIS

One Platform, Two Simulation Technologies.



SIMetrix/SIMPLIS combines two complementary simulation engines in a single integrated environment.

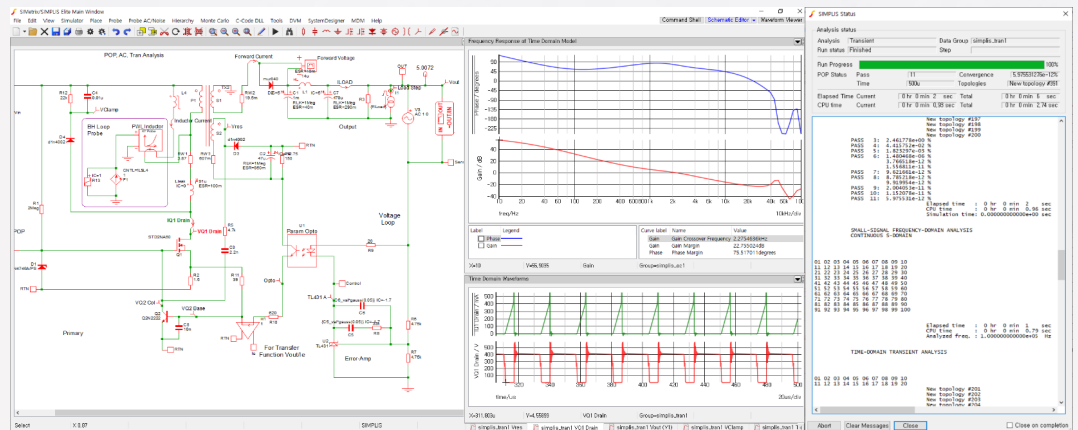
SIMetrix

A powerful SPICE simulator for analog, digital and mixed-signal circuit simulation.

SIMPLIS

Piecewise Linear simulation for Switching Power Electronics.

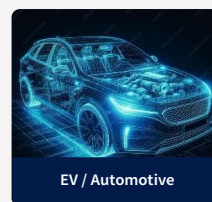
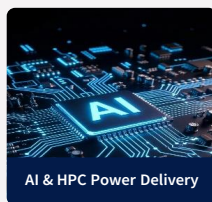
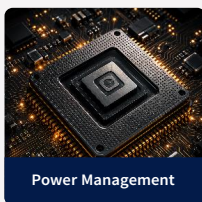
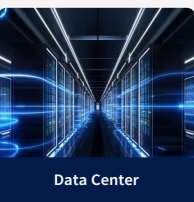
POP analysis enables steady-state and AC analysis without requiring averaged models.



Why Choose SIMetrix/SIMPLIS?

- ✓ **Fast Simulation**
Reduce simulation time and accelerate design iterations.
10-50x faster for switching circuit simulation
- ✓ **Accurate Results**
Circuit-level accuracy for reliable design verification.
- ✓ **Integrated Workflow**
Two complementary simulators in one environment.
- ✓ **Vendor-Provided Simulation Models**
Leading semiconductor manufacturers provide simulation models for SIMetrix/SIMPLIS.

Typical Applications

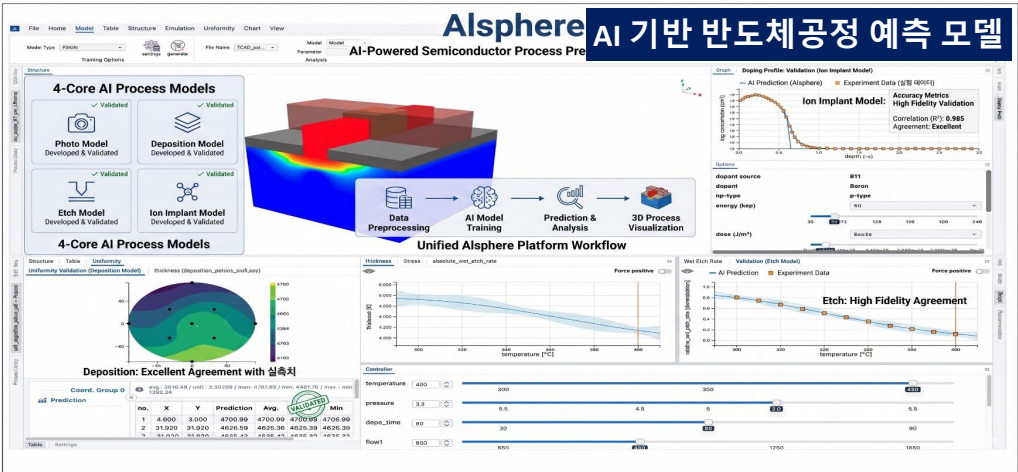
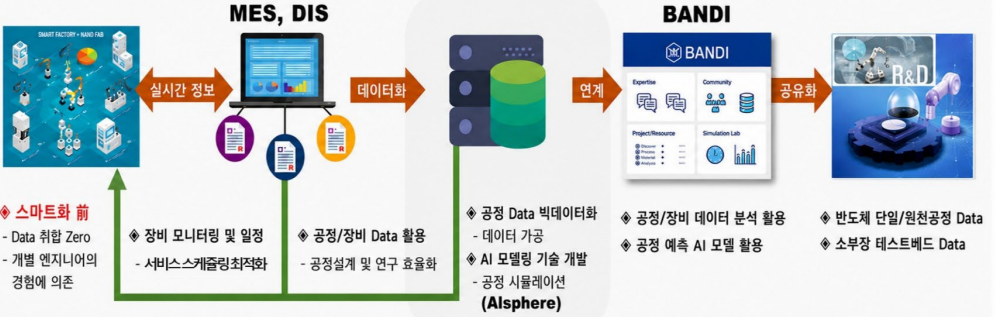


AI·데이터 기반 나노패 공정 스마트 서비스 사업

나노패 스마트화를 통한 기능 및 서비스 고도화

하드웨어+소프트웨어

공정 빅데이터화 및 AI 활용 디지털화(BANDI 연계)

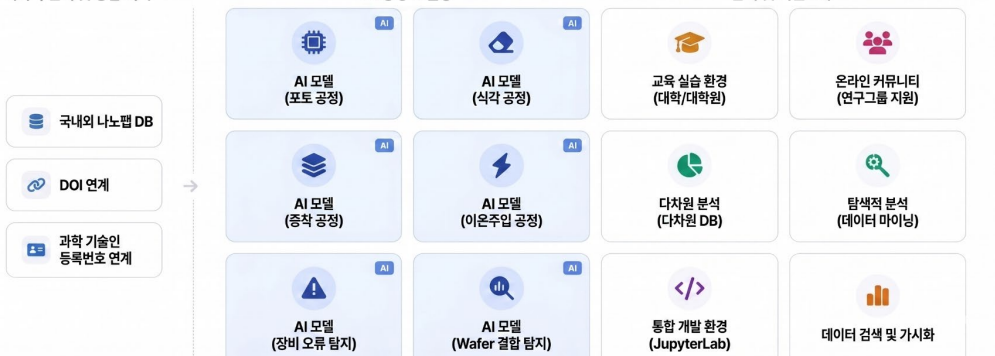


AI 기반 반도체 공정 및 장비 데이터 공유 플랫폼 BANDI

데이터 연계 및 통합 서비스

AI 공정 모델링

분석 및 지원 도구



SoC 설계 및 하드웨어 가속 검증 플랫폼

ULTRON II



ULTRON II는 AMD ZYNQ UltraScale+ MPSoC 기반의 고성능 임베디드 개발 플랫폼입니다.

하드웨어 가속화를 위한 이기종 컴퓨팅 아키텍처를 기반으로 **AI 가속, 자율주행, 5G, 자동화 산업** 등의 첨단 기술 개발 환경을 제공합니다.



■ SoC 기반의 FPGA 하드웨어 가속화 지원

- AMD 16nm ZYNQ UltraScale+ MPSoC 적용
 - Quad Core ARM Cortex-A53
 - Dual Core ARM Cortex-R5F
 - ARM Mali-400MP2 GPU
 - 600K Logic Cell 지원

■ 편리한 개발 환경

- Low Level 설계
 - VIVADO Design Suite
- High Level 설계
 - VITIS, VITIS HLS, VITIS AI

■ 다양한 확장 Interface 지원

- FMC (FPGA Mezzanine Card) Connector 제공
 - LCD/CAM Module 활용 가능
 - Header Pin Card 활용 가능
- Pmod (Peripheral Module) Connector 제공

■ 사용자 중심의 실습 Contents 제공

- 사용자를 위한 다양한 실습 Contents 제공
- 실습 및 연구개발을 위한 기술 지원

Libertron

Alliance Program
Certified Member

Authorized
Training Provider

AMD VARs
(ALVEO Formal Supplier)

University Program
Partner

AMD

FPGA & 임베디드 AI 시스템 설계 전문 기업

[주]리버트론

sales@libertron.com | TEL. (02)3486-5278 | FAX.(02)3486-5271 | www.libertron.com
서울특별시 영등포구 당산로 41길 11, 당산 SK V1 Center W동 1111호 (우편번호) 07217

LX Semicon offers differentiated value to customers with constant challenges and innovations, and is moving forward to become a global leading system semiconductor company.



Display Solution

- ✓ Display Driver IC
- ✓ Mobile Driver IC
- ✓ Timing Controller
- ✓ Power Management IC
- ✓ Touch IC



Automotive Solution

- ✓ Micro Controller Unit
- ✓ Motor Driver IC
- ✓ Interface IC
- ✓ Metalized Ceramic Substrate
- ✓ Display ICs



Home Appliance Solution

- ✓ Micro Controller Unit
- ✓ Motor Driver IC

TENSOR™

MS46600A ————— UP TO 43.5 GHz

When measurement
defines the future

정밀성 / 안정성 / 신뢰성



제품 상세 보기

세계 최초 AI 탑재
벡터 네트워크 분석기



주요 특징

■ 포트별 독립 소스

각 포트별 소스 기본 제공

■ AI 기능 기본 탑재

자체 LLM 기반 AI 기능 기본 탑재

■ 초고속 측정 - 5 μ s/point

매우 빠른 측정 속도

■ 송수신 위상 동기

2nd LO 옵션으로 송수신기가 위상 동기된 조건에서
Vector Mixer 측정 등 고난도 측정 가능

■ UltiCal™ 자동 교정

세계 최초 43.5 GHz 4-port 자동 Cal 지원

고성능 스마트 PMIC 기업, 실리콘마이터스

반도체 설계전문가 집단 실리콘마이터스는 고성능/고효율 스마트 PMIC(전력관리 통합칩)의 상품기획, 개발, 제조를 하는 팹리스 회사로서 이를 통해 스마트폰 및 Tablet TV, 노트북, 모니터, Auto motive, IoT 등 다양한 전자제품에 최적의 전력관리 솔루션을 제공합니다.



“더 나은 세상, 더 즐거운 생활을 함께 만들어 나갈 인재를 찾습니다.”



Silicon Mitus



QRT's COTS Reliability Testing

Upscreen for aerospace/satellite application

QRT's **ONE-STOP** Upscreen Service

- ✓ Designed for NewSpace's Low-Cost Needs
- ✓ Proprietary SEE/RF Technology
- ✓ Industry-Leading Expertise in Reliability and Failure Analysis

QRT One-Stop Solution :

Automotive Electronics Qualification

- NewSpace COTS components primarily adopt Automotive COTS, ensuring cost-efficiency and availability
- AEC-Q100 Qualified Testing



Soft Error & Radiation Test

- Space radiation resilience validation
- Soft error rate analysis
- Total Ionizing Doses effect (TID) analysis

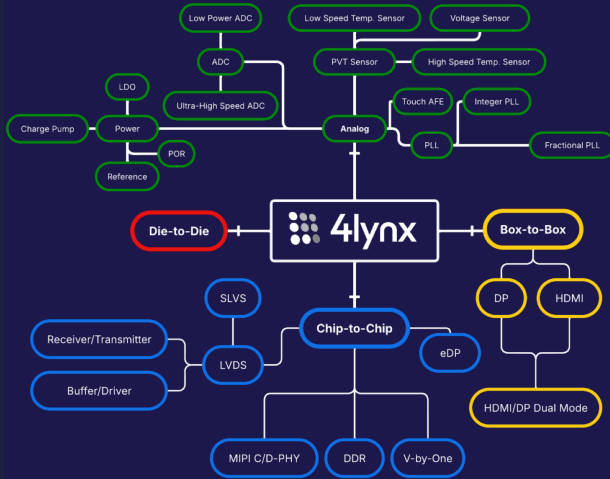
RF HTOL Life Test

- Validates performance under real RF operating conditions.
- Temperature-dependent lifetime predictions
- Drain-voltage characteristic analysis



DPA (Destructive Physical Analysis) & CA (Construction Analysis)

- Failure Prevention & Structural Integrity Check
- Reference : MIL-STD-1580, MIL-STD-883, RoHs, MIL-STD-750



(A, B, C, D) Core IP Categories:

Analog IP: PLL, ADC, PVT Sensors, LDO, POR

Box-to-Box: HDMI, DisplayPort, eDP

Chip-to-Chip: LVDS, MIPI C/D-PHY, DDR, V-by-One

Die-to-Die: UCIe

Worldwide Provider
to US, CN, JP, KR...Foundry Experience
IP solutions down to 2nm GAAMixed-signal Excellence
FinFET/GAA expertise16+ Years of Interface IP
Founded in 2010

모 집 부 문

아날로그 설계 엔지니어

Full Custom
레이아웃 엔지니어

RTL 설계 엔지니어

지원자격

- 경력: 무관 (신입 지원가능)
- 우대:
 - 아날로그 IC 설계 유경험자
 - 석사 학위자
- 전문연구원 가능

담당업무

- HDMI, DisplayPort, MIPI 등 고속 IP 설계
- PLL, CDR, CTLE, DFE, ADC, DAC 등 SerDes 구성 회로 설계

지원자격

- 경력: 무관 (신입 지원가능)
- 우대:
 - 아날로그 IC 설계 유경험자
 - 석사 학위자
 - Virtuoso / Calibre 유경험자

담당업무

- Full Custom Layout
- Physical Verification: LVS / DRC / ERC / DFM

지원자격

- 경력: 무관 (신입 지원가능)
- IC 설계 Flow 및 설계 방법론에 대한 이해
- Verilog / SystemVerilog를 활용한 RTL Coding & Simulation 가능자
- 우대:
 - 아날로그 IC 설계 유경험자
 - 석사 학위자
 - FPGA 설계 경험자
 - C/C++, Script Language (shell/tcl) 가능자
 - RTL 합성 및 Timing 분석 가능자
 - 전기/전자공학 전공자

진원과 회사가 함께 성장 할 수 있는 비전을 가지고 성장해온 회사입니다.

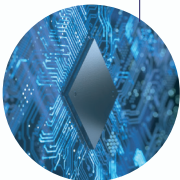
특히 구성원 각각의 자율과 역량을 기반으로 개인의 능력을 펼칠 수 있는 환경을 제공하고 있습니다.

엔지니어링에 진심이며 자체 OJT 프로그램을 통해 시·최신 기술 습득 및 시·반도체 설계 엔지니어로 발전할 수 있는 기회를 제공하고 있습니다.

“ AI/Soc 임베디드솔루션을 선도하는 R&D 중심의 전문 기업 ”

반도체 검증 핵심 기술

SoC 설계 검증
반도체 RTL 설계 검증
FPGA 기반 Prototyping
ARM Core 인터페이스
PCIe, DRAM, MIP, USB3.0 기술



임베디드 & AI 솔루션

시스템 솔루션(운영체제, BSP)
카메라 시험 모듈
Linux, Embedded, FPGA 원천기술
딥러닝, 사물인터넷, 자율주행, 장애물회피



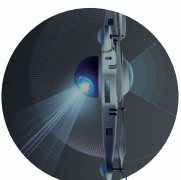
ARM 소프트웨어

ARM(세계 1위) 임베디드 소프트웨어
전자 기기 핵심 코어 설계 검증 소프트웨어
IoT, 인공지능 설계 소프트웨어



글로벌 Top Class AI 드론

드론체계 종합기업
드론관계 시스템, 관계 스테이션
드론 다중운용 시스템
특수임수 탑재



나인플러스 IT(주)는 **Cadence®**의 **한국 공식 채널 파트너**로서, 전기·전자·반도체·기계 등 전 산업 분야에 걸쳐 고객의 요구에 최적화된 **Total Engineering Solution**을 제공합니다.

당사의 폭넓은 제품 포트폴리오를 통해 고객 비즈니스의 혁신과 성장을 적극 지원합니다.

2009년 창립 이래, 나인플러스IT(주)는 다양한 기업, 연구 기관, 교육 시설에 Cadence® 소프트웨어를 공급하면서, 전문적인 컨설팅, 신속한 기술 지원, 그리고 체계적인 교육 서비스를 지속적으로 제공해 왔습니다.

또한, 저희는 자체 교육장을 운영하여 정기적인 교육 프로그램을 진행하고 있으며, 다양한 협력 기관 및 학회와의 연계를 통해 특강도 주기적으로 제공하고 있습니다. 미래 인재 양성에도 깊은 관심을 기울이며, 다양한 경진대회를 주관하여 산업 발전에 적극적으로 기여하고 있습니다.

-  협약을 통한 맞춤 사업
-  소프트웨어 공급
-  교육 서비스 제공
-  엔지니어링 컨설팅 & 기술지원

cadence®

Cadence®는 지난 30년간 **Electronic Design Automation(EDA)** 분야의 **선두 주자**로서 독보적인 입지를 구축해 왔습니다.

산업과 기술의 경계가 허물어지고 융합 기술 및 서비스가 중요해짐에 따라, Cadence®는 설계 및 해석 소프트웨어를 넘어 하드웨어와 IP 분야에 이르기까지 고객 만족을 극대화할 수 있는 다양한 서비스를 제공하고 있습니다. 일반 소비자용 제품부터 하이퍼 스케일 컴퓨팅, 5G 커뮤니케이션, 자동차, 항공, 헬스케어 등 광범위한 산업 분야에서 필수적인 칩, 보드, 시스템을 위한 최적의 솔루션을 제공합니다.

SW, HW,
& IP
for Chip and
System Design

Serving
Semis &
Systems
Customers

~11,000
Employees
in 25 countries

~9,000 in
Engineering

35%
Revenue
Invested in
R&D

Fortune 100
Great Places
to Work

9 years
in a row

* 2022년 12월 31일 기준

서울본사

주소 서울특별시 금천구 가산디지털2로 144
현대테라타워 가산DK 705-706호
TEL 02-867-8633
FAX 02-867-8632

E-Mail info@npit.co.kr

부산지사

주소 부산광역시 해운대구 센텀중앙로 90
큐비@센텀 1602호
TEL 051-758-4841
FAX 051-758-4866

Web www.npit.co.kr

아카데미

주소 서울특별시 금천구 디지털로 121
에이스가산타워 203, 204호
TEL 02-3016-7926
FAX 02-3016-7927

Web www.nescampus.co.kr



VITAL IC.CO.LTD

A specialized fabless semiconductor company for intelligent bio-signal processing, supplying high-performance, low-power analog signal-processing chips combined with Tiny ML algorithm technology, optimized for biomarker and vital-sign monitoring.

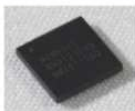
Company Profile

Company Name	VITAL-IC Co., Ltd.
CEO	Wang Seong-ho
Date of Establishment	Oct. 16, 2017
Employees('25)	22
Location	701-4, C-dong, 242 Pangyo-ro, Bundang-gu, Seongnam-si, Gyeonggi-do (Pangyo Digital Center)
Standard Industrial Classification	C26129 (Manufacture of Other Semiconductor Devices)
Listing Status	Unlisted
Capital ('25, USD)	459,900

Semiconductor Chips

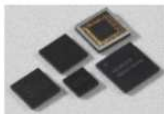


NMX1111

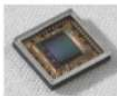


NMX4110

Chip Portfolio



Bio-signal Chips



Inside the Chip

Application Modules



A1000



C1000



E1000



P1000

Business Overview

○ Key Business Areas

- Vital-sign monitoring: CGM, ECG, EEG, respiration, etc.
- POCT (Point-of-Care Testing): malaria diagnostic kits, etc.
- Wearable devices: smartwatches, smart rings, etc.

○ Technology / Service Introduction

- Key Products
 - NMS4110 – Electrochemical ROIC for CGM, ECG, EEG
 - NMS4150 – Bio-signal processing SoC
 - NMS1111 – Multi-modal chip for smartwatches and smart rings
- Key Technologies
 - High-resolution, low-power analog semiconductor design technology
 - Tiny ML algorithm technology for on-sensor AI
 - Ultra-compact, low-power single-chip integration technology

○ Market Size & Outlook

- Digital Healthcare Device Market
 - Global market projected to reach US\$35 billion (approx. KRW 52 trillion) by 2035, at a CAGR of 18.9%
 - CGM shipment volume surpassed 350 million units in 2025; the sleep-monitoring device market is now growing rapidly as well
 - Having overcome the "pilot trap" of the early 2020s, demand for healthcare devices is growing quickly
- Point-of-Care Testing (Diagnosis) Market
 - Global POCT market valued at US\$44.1B in 2025, projected to reach US\$85.2B by 2035
 - Infectious-disease testing is a key segment, though growth has been limited by sensitivity, cost, insurance and data-interoperability issues
 - Advances in high-resolution electrochemical bio-signal processing and on-device AI are expected to rapidly expand point-of-care diagnostics for infectious diseases

Investment Highlights

○ Fundraising Status

- Raised a cumulative KRW 10.3 billion from institutional investors, including Capstone Partners

○ Awards and Certifications

- ISO 9001 (Quality Management System, Oct. 2023)
- QRT Reliability Certification
- Citation from the Minister of Trade, Industry and Energy (2024)

○ Key Partnerships and Collaborations

- Development agreement with Company W for a CIS chip for capsule endoscopy
- Organoid development collaboration with Johns Hopkins University (JHU)
- PoC with K-water (Korea Water Resources Corporation) for a harmful-bacteria monitoring solution

UXF

DEEPX

초저전력·초저발열 기술로 운영비까지 혁신적으로 낮춘 온디바이스 AI 반도체.
딥엑스의 차세대 NPU 솔루션으로 비즈니스 효율을 극대화하세요.



DEEPX Physical AI Products Line-up



DX-M1
M2. Module



DX-M1M
M2. Module



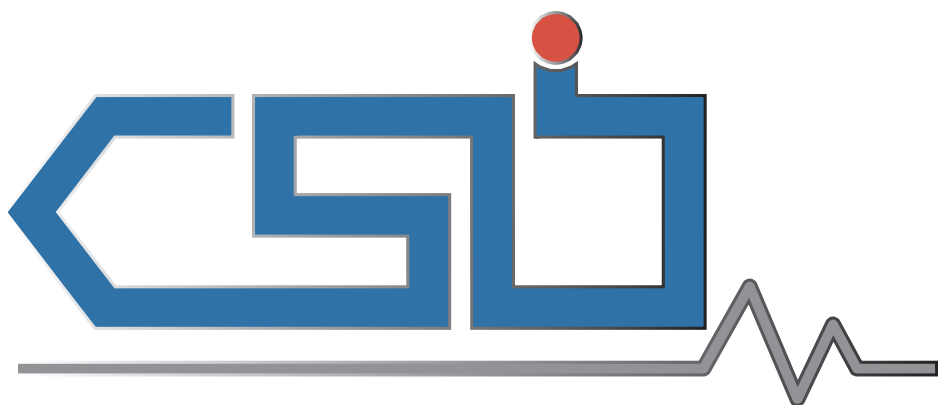
DX-AIPlayer
AI Edge Box



DX-H1 Quattro
PCIe Card



DX-H1 V-NPU
PCIe Card





AI 반도체 프로세싱 SW 연구센터
AI Semiconductor Processing SW
Research Center



INHA UNIVERSITY

인공지능 시스템반도체 연구센터

대규모데이터센터용 인공지능시스템반도체 연구센터



연구센터 소개

연구명

초거대 AI를 위한 대규모데이터센터용 인공지능 시스템반도체 인력 양성 및 핵심기술 개발

연구내용

- 대규모 네트워크 경량화 및 최적화 설계
- 데이터처리용 전력변환회로 및 인터페이스 설계
- 최적 구조 메모리 어레이 개발
- 저전력 고효율 시넵스 소자 및 구동회로 개발

참여인력

참여 연구자 총 116명

- 대학교수 10명
- 전임연구원 2명
- 석사 70명 / 박사 34명

참여 대학 5개, 참여 기업 16개

참여 대학



참여 기업



연구 개발 및 인력 양성 목표

최종 연구 목표

초거대 AI를 위한 대규모데이터센터에 활용될 수 있는 초고효율 · 초저전력 인공지능 반도체 핵심 기술 개발 및 고급 인력 양성
(수혜인원: 총 600명, 배출인원: 총 480명)

연구센터의 핵심 목표

- 인공지능 반도체를 위한 시스템 핵심/응용 SW 기술과 회로/소자 핵심 설계 및 융합 기술 개발
- 초거대 AI를 위한 대규모데이터센터에 활용 가능한 인공지능 반도체 플랫폼 연구 개발
- 인공지능 반도체 관련 소프트웨어와 하드웨어 설계 역량을 갖춘 SW-HW 융합형 석·박사 고급 인력 양성
- 산업체 수요 중심의 실증적 연구와 창의/융합형 인재 육성을 통한 인공지능 반도체 분야의 선도적인 연구센터 운영

주요 연구 내용

- 대규모 멀티모달 네트워크 시스템 경량화 설계 및 최적화
- 대규모서버용 Storage 메모리 소자 개발
- 고효율 전력변환회로/고속 ADC 및 Interface 설계
- 저전력 고효율 시넵스 소자/어레이 개발

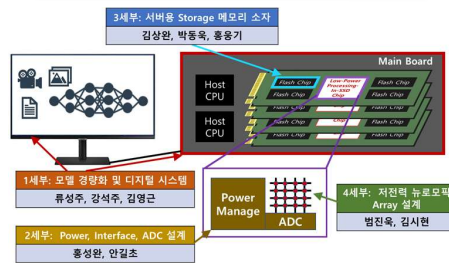
세부 연구 개발 목표

데이터센터의 고효율 인공지능 시스템을 위한 Processing-In-SSD SW/HW 플랫폼 설계

인공지능시스템을 위한 데이터센터용 고효율 전력변환 및 고속 인터페이스 설계기술개발

데이터센터를 위한 저전력 차세대 반도체 소자 기술 개발

데이터센터용 저전력 고효율 인공지능 연산을 위한 시넵스 어레이 개발



산학밀착형 양방향 인력양성 시스템 구축



산업체 고용연계 추진 계획



산업체 장/단기 인턴십 운영



아날로그 RF회로 및 시스템 연구센터

● 센터소개

- ▶ 본 센터는 EMI/EMC, 밀리미터파 IC 설계, 초고주파 IC 설계, RF 전력증폭기 설계, 전력 IC 설계, 인공지능 IC 설계, 고속 인터페이스 IC 설계, 안테나 해석 및 설계 등과 같은 세부 연구분야로 구성
- ▶ 국내 유일의 고속 IC의 설계 및 시스템의 제작, 그리고 전기장에 대한 노이즈 해석 및 최적화를 단일 센터 내에서 할 수 있는 올인원 시스템을 갖추고 RF 및 고속 시스템 해석을 위한 인프라를 최고로 효율적인 수준으로 유지 관리 하는 것을 목표로 함

● 교수진



서문교 교수



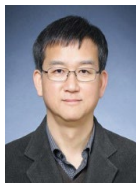
강태욱 교수



김병성 교수



김소영 교수



나완수 교수



박준은 교수



박형원 교수



양영구 교수



유창식 교수



이강윤 교수



이우근 교수

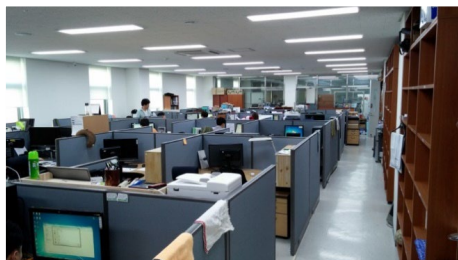


조건희 교수



황금철 교수

● Open Lab



성균관대학교
SUNGKYUNKWAN UNIVERSITY(SKKU)

| 아날로그 RF회로 및 시스템 연구센터

<http://arrc-skku.co.kr/>



지능형 의료 영상 진단 솔루션 연구센터

센터 컨소시엄

지능형 의료 영상 진단 솔루션 연구센터

혁신도약학과제

1 세부 지능형 진단 및 AR 기반 시각화 시스템 개발

세부책임 | 아주대 선우명훈 교수
지능형 진단 딥러닝 최적화 및 연산 엔진 연구

서울대 이혁재 교수

AR 기반 시각화 시스템 개발

아주대 박성준 교수

피부적합형, 체내 삽입형 전자/광소자 개발

+ 아주대병원 김태희 교수
+ 아주대병원 하태양 교수
유방암 공동연구

+ 아주대병원 정우영 교수
호흡기 질환 공동연구

NCKU Gwo Giun Lee 교수

피부암 검출 및 SoC 연구

2 세부 영상/임상 빅데이터 융합 진단 모델 개발

세부책임 | 아주대 이정원 교수
학습 데이터 품질 기반 진단 모델 검증

연세대 고정길 교수

학습 기반 의료 영상 분석 시스템 연구

포항공대 김원하 교수

MRI 기반 딥러닝 처리 연구

+ 아주대병원 선준성 교수

폐 질환 공동연구

OUS Mi Zhang 교수

의료 데이터 분석 연구

3 세부 뇌 영상 및 생체 신호처리 기술 개발

세부책임 | 연세대 김동현 교수
딥러닝/영상시스템 기반 진단 모델 개발

포항공대 이영주 교수

생체 신호처리 압축 센싱 복호 기법 연구

한국과학기술원 예종철 교수

의료영상 처리 연구

+ 서울의료원 최현석 과장

뇌 질환 공동연구

UC 버클리 Chunlei Liu 교수

뇌 MRI 진단 연구

4 세부 의료용 동적환경 3D 재구성 연구

세부책임 | 아주대 구형일 교수
의료 영상 비강제 3D 재구성 연구

+ 아주대병원 김진홍 교수
+ 아주대병원 양민재 교수
소화기 질환 공동연구

칭화대 Hua Guo 교수

MRI 영상 재구성 연구

■ ICT 관련 교수
■ 의대 교수
■ 해외 대학 교수
■ 컨소시엄 기관

에디테크놀로지

라온텍

인피니트헬스케어

네모누리

딥노이드

자람테크놀로지

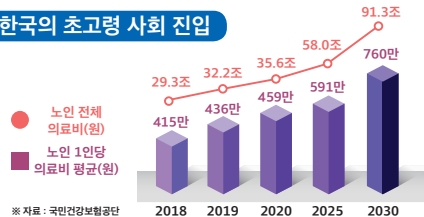
제이엘케이

에스앤지바이오텍

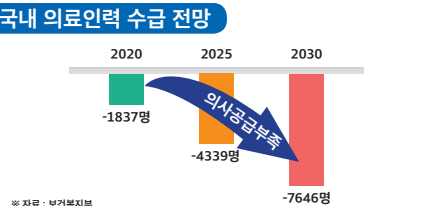


지능형 의료 영상 진단 솔루션 개발

한국의 초고령 사회 진입

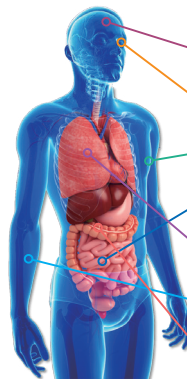


국내 의료인력 수급 전망



지능형
의료 영상
진단
솔루션

MIIDS Research Center
AJOU Univ. 아주대학교
Medical Image-Based
Intelligent Diagnosis Solution



뇌질환 MRI / EEG

황달/치매 스마트폰 카메라

유방암 X-ray

소장 캡슐내시경

폐 CT / X-ray

골절 CT

복부 CT

HYPER ACCEL WE'RE HIRING!

우리는 LLM 서비스에 특화된 고효율 AI 반도체를 개발하며,
기업과 개인이 LLM을 지속적으로 이용할 수 있는 컴퓨팅 인프라를 실현합니다.

신입 / 경력 개발자 채용



접수 방법 : 홈페이지 지원 QR 참조 ↑
근무지 : 강남 뱅뱅 사거리



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